POWER FACTOR IMPROVEMENT AND HARMONIC REDUCTION IN THYRISTOR CONVERTERS

A Thesis Submitted
in Partial Fulfilment of the Requirements
for the Degree of

DOCTOR OF PHILOSOPHY

By
H. K. PATEL

to the

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CERTIFICATE

Certified that this work, 'POWER FACTOR IMPROVEMENT AND HARMONIC REDUCTION IN THYRISTOR CONVERTERS' by H.K. Patel has been carried out under my supervision and that this work has no been submitted elsewhere for a degree.

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H.K. Patel

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a_n, b_n	Fourier coefficients
$B_1, B_2, \ldots B_m$	Pulse positions
d	Half pulse width
e, e_s	Instantaneous line voltage
E_m	Maximum line voltage
i_a	Instantaneous load current
I_{ar}	Amplitude of reactive component of the load current
I_{aw}	Amplitude of active component of load current
i_d	Instantaneous output current of the converter
I_d, I_{dav}	Average output current of the converter
I_m	Maximum line current
I_{rms}	RMS line current
L	Inductance of thyristor-controlled reactor
M_{af}	Mutual inductance between armature and field
n	Order of the harmonic
P	Number of pulses (chops) per half cycle of the line voltage
q	Instantaneous value of the normalised reactive power of the converter
r	Normalised average output voltage of the converter (output voltage ratio)
R	Load resistance
S	Speed of the motor
$t_1, t_2, \ldots, t_m$	Tap ratios

v_d Instantaneous dc voltage of the converter

V_d Average value of the dc voltage

$\alpha_1, \alpha_2, ..$ Turn on angles

$\beta_1, \beta_2 ..$ Turn off angles

SYNOPSIS

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Rapid progress in thyristor control technology has given rise to increasing uses of thyristor converters (ac-dc converters and ac-controllers) for power control in ac and dc applications. They offer numerous advantages such as higher efficiency, better reliability, fast time response and compact size. Although, most of the applications employ naturally commutated phase-controlled converters because of their reliability and simplicity they suffer from the limitations of generation of line current harmonics and poor power factor at low output voltages. Line current harmonics cause interference with communication lines and adversely affect the performance of other devices operating on the same lines. Similarly, the operation of the system at low power factor results in reduction of power transfer capability of the transmission lines and increase of system

losses. These problems are most vital in electric traction systems due to relatively weak lines. As a consequence of ever increasing demand of thyristor converters, the problems associated with the converter-utility interfacing are of primary concern in order to maintain the quality of the supply and the efficiency of power transmission.

Although, the problems posed by the thyristor converters may be overcome by employing harmonic filters and reactive power compensator externally, their uses have been restricted due to increase in system cost. Hence, in recent years, attempts are being made to improve the converter performance through the use of better and sophisticated converter controls.

A number of improved methods of converter control, based on natural as well as forced commutation, have been developed for the harmonic reduction and power factor improvement of the converters. However, the use of improved phase-control scheme (controlled flywheeling) in ac-dc converter control and the concept of harmonic elimination in ac-dc converters and ac-controller are not fully explored.

In the recent years, the static compensators using thyristor-switched capacitors (TSC) and thyristor-controlled reactors (TCR) find extensive use for dynamic compensation of load reactive power. They have all the advantages listed above for the thyristor converters. Like the converters, the static

VAR compensators employing thyristor-controlled reactor also suffer from the problem of generation of line current harmonics. Though the operation and applications of static VAR compensators are well covered in the literature details of the control circuits and the harmonic control in TCR have not been emphasised.

The objective of the work reported in the thesis are :

1. Detailed evaluation of existing control schemes both in ac-dc converters and ac-controllers.
2. Development of sequence control scheme for ac-dc converters employing controlled flywheeling technique.
3. Development of control schemes for selective harmonic elimination in ac-dc converters and ac-controllers.
4. Development of control schemes for static VAR compensators for power factor correction and harmonic reduction in thyristor-controlled reactor.

The major contributions of the thesis are as follows :

1. Comparative study of existing control schemes of single-phase ac-dc converters and ac-controllers is carried out for determining the relative merits of one scheme over the other.
2. Improved sequence control scheme for single-phase line-commutated converter is proposed which reduces the reactive power consumption as well as line current harmonics.

3. Selective harmonic elimination methods for ac-dc converters and ac-controllers are proposed. Power circuit for ac-controller and control circuits for ac-dc converter and ac-controller are developed.

4. Control schemes for TSC and FC-TCR compensators are developed for power factor improvement. Two control strategies for thyristor-controlled reactor are proposed for minimization of reactor current harmonics.

An outline of the work reported in the thesis is given below :

1. Chapter 1 introduces the various aspects studied and reviews the literature in this area.

2. Chapter 2 deals with a comparative study of control schemes for natural- and forced-commutation control of single-phase AC-DC converters. Assuming a smooth load current and an ideal commutation, the comparison is carried out on the basis of system power factor, fundamental reactive power, distortion factor, voltage ripple in the output voltage, dominant line current harmonics etc. Further, the influence of two modulation schemes, namely, symmetrical pulsewidth modulation and asymmetrical pulsewidth modulation, on the motor performance and on the source is investigated for their comparison.

3. An improved sequence control for series connected bridges with graded ratings is described in Chapter 3. A generalised method for selecting the ratings of the bridge converters and two control strategies for minimizing the reactive power are described. Converters are operated with the half-controlled characteristics.

4. Chapter 4 deals with the selective harmonic elimination in the forced-commutated single-phase ac-dc converters. A pulse-width modulation scheme is described for the elimination of one or more unwanted line current harmonics. In that, the pulses are of equal widths and they are arranged symmetrically around $\pi/2$ axis of the supply voltage for a unity displacement factor. The locations of the pulses depend upon the harmonics to be eliminated. A generalised algorithm is developed for determining the pulse positions.

5. Chapter 5 presents a comparative study of different control schemes for single-phase ac-controllers feeding a resistive load. Comparison is based on the performance criteria such as line current harmonics, system power factor distortion factor and displacement factor.

6. Chapter 6 deals with selective harmonic reduction in ac-controllers feeding resistive load, making use of pulse-width modulation scheme. To keep the displacement factor unity pulses in a half-cycle are arranged to be symmetrical about the $\pi/2$ axis.

To reduce the undesirable line current harmonics, suitable pulse-positions are determined. Power variation is achieved by varying the pulse-widths symmetrically around the pulse positions.

A general method of eliminating M number of harmonics is discussed. An algorithm relating the pulse positions and the harmonics to be eliminated is presented. Power and control circuits to implement the scheme are discussed.

The harmonic elimination method is not applicable for the elimination of any one harmonic, excepting the triplen harmonics. However, with the assumption of flat-topped current waveform, pulse positions are determined for minimization of any one line current harmonics.

7. Chapter 7 deals with static VAR compensators for power factor correction. Principles of transient free switching of capacitor bank are described and a control scheme for thyristor-switched capacitor compensator is presented. Operation of fixed capacitor- thyristor-controlled reactor (FC-TCR) type compensator is described. A digital control scheme for FC-TCR compensator for power factor correction is described.

To reduce the harmonics generated by TCR, two sequence control schemes for thyristor controlled reactor are developed.

8. The concluding chapter outlines the conclusions drawn from the thesis and gives suggestions for further work.

CHAPTER 1

INTRODUCTION

1.1 GENERAL

Thyristor converters (ac-dc converters and ac controllers) are widely used for power control in ac and dc applications because of high efficiency, fast response, less maintenance, compact size, quiet operation etc. However, they pose two major problems, viz., generation of line current harmonics due to non-sinusoidal converter current and poor power factor. These problems are more acute with the naturally commutated converters which are mostly preferred because of their ruggedness and simple control. Harmonic currents may cause 1) erroneous operation of the regulating and control systems operating on the same power lines, 2) noise generation in the neighbouring communication networks, 3) excessive heating and torque pulsations in the rotating machineries, and 4) resonance between the power factor capacitors and system reactance at harmonic frequencies. Filtering of lower order harmonics will need a large size filter which in turn will increase the cost and power losses. Therefore, harmonics of lower order deserve more attention than the higher order. Likewise, the low system power factor increases transmission losses and reduces the power transfer capability of lines due to affected voltage regulation.

As a consequence of ever increasing demand of thyristor converters, which now form a significant part of the total load, greater attention is being paid to the problems existing in the converter-utility interface. The magnitudes of the harmonics and the reactive power in the converter depend much upon the converter control scheme. Many methods, based on natural and forced commutations, have been investigated for power factor improvement and harmonic reduction in the converter. These methods reduce the cost of the harmonic filters and the reactive power compensators used for external compensation.

The recent development of static reactive power (reactive volt-ampere-VAR) compensators has brought remarkable improvements in the generation of controlled reactive power. Their ability to provide dynamic compensation in response to the changing system conditions can result in numerous improvements in industrial and power system performance depending on the control objectives. Few of them are cited below :

1. Reduced voltage flicker due to irregular load fluctuations.
2. Power factor improvement and load balancing.
3. Increased transient stability and transmission line power transfer capacity.
4. Improved system dynamic stability due to increased system damping.

5. Improved transmission system efficiency.

6. Control of steady state and transient overvoltages.

The main theme of this thesis is to develop suitable control schemes for ac-dc converters and ac controllers for power factor improvement and harmonic reduction. Before discussing the work reported here, a brief review of relevant literature is taken up.

1.2 POWER CONTROL IN THYRISTOR CONVERTERS

Due to simplicity in control, thyristor converters in most of the applications are phase-controlled. However, phase control has the disadvantages of poor power factor and generation of high magnitudes of lower order line current harmonics [1-3]. In the near future, the harmonic pollution in the power systems, due to ever increasing use of thyristor converters, will be of serious concern unless the measures are taken for harmonics reduction. Details on the harmonics effect and permissible maximum harmonic distortion are given in Ref.[1]. In the following sections, the different control schemes for performance improvement of single phase converters are reviewed.

1.2.1 Control of ac-dc Converters

In industry and electric traction, thyristor converters are extensively used for control of dc motors. Regenerative operation employs fully-controlled converters which are generall

phase-controlled. However, as mentioned above, this method yields poor power factor and higher ripple content in the armature current which introduces commutation problems in dc motors [4].

Line Commutation :

Sequence control of two or more bridge converters in series improves the power factor and reduces the load current ripple [5-6]. Here, for adjustable output voltage, one bridge is phase-controlled while others are maintained at full advance or full retard. McMurray [6] has shown that by asymmetrical triggering of bridge converter, i.e., a pair of thyristors initially maintained at fixed triggering angle, generally full advance or full retard, while the other pair phase controlled, power factor can be improved. However, in this method, line current will contain a d.c. component which is not a desirable feature. He has also shown that this method is not suitable to single three phase bridge converter, because it generates third harmonic ripple in the output voltage and second harmonic component in the line current. Mehta et al. [7] have investigated the performance of dc motor with asymmetrical control of single stage and multistage single phase bridge converters and had shown that though the power factor is improved the steady-state and transient responses of the drive are inferior to that of conventional phase control

triggering. Mukhopadhyay [8] has presented a scheme for optimal reactive power in sequence controlled bridge converters using conventional phase-control. Ohnishi et al. [9-10] have presented a bias voltage control scheme for power factor improvement in single phase and three phase converters for rectification operation. It involves large number of semiconductor elements. Farrer et al. [11 - 12] have presented an improved phase control scheme which permits the fully controlled converter to operate with half-controlled characteristic. In this, the negative and positive pulses in the output voltage during rectification and inversion respectively are eliminated by controlled flywheeling operation of the converter.

Forced Commutation :

The use of force-commutated thyristor converter as a means of controlling reactive power and line current harmonics has been shown to have considerable promise. By operating the converter with appropriate multiple pulse-width modulation, the reactive power can be reduced to zero and the harmonic spectrum can be shifted to higher order to any desired extent. The resulting improvement in the converter performance may justify the added expense of commutation circuit and the complexity of the control. However, the gate turn-off (GTO) thyristors when available will simplify the control and power circuits of force-commutated converters by obviating the need of commutation circuits.

Sen et al. [13] have investigated extinction angle control and symmetrical pulse-width modulation (SPWM) schemes for improvement of power factor and motor performance. In the former, the fundamental power factor has leading value. The power circuit used by them consists of an uncontrolled bridge rectifier and a chopper in the output circuit. In Ref. [14], a current limit control scheme have been investigated. In this, when the armature current exceeds a set maximum limit, motor is disconnected from the supply and the motor current is allowed to freewheel. Next, when the motor current falls below a set minimum current, the motor is again connected to the supply by turning the chopper on. The power circuit is the same as said above. In Ref. [16], a SPWM technique has been investigated for three-phase bridge converter, and a converter circuit consisting of thyristor bridge converter and a chopper in the output circuit for regenerative operation has been presented. Kataoka et al. [17] have investigated the converter performance with a sinusoidal modulation, and have presented a versatile converter circuit which is capable of regenerative operation and does not require auxiliary thyristors for force commutation.

The presence of third harmonic generated by the thyristor systems worsens the quality of the supply which causes the temperature rise and system resonance of power capacitors and malfunctioning of system protective relays. To prevent the interference of higher harmonics with the communication lines, filters

must be used. In certain cases, where the filters are installed for this purpose, efforts to reduce the higher order harmonics have resulted in the shift of resonance frequency, between circuit constants of the line and those of the filter components, towards the lower harmonic range. This causes further increase in the third harmonic current on the part of the electric power system.

For third harmonic reduction, Matsuhashi [18] has suggested sequence control of two series connected bridges, one uncontrolled and other controlled with ac chopper in its input. SPWM control with one pulse per half cycle has been used. Zander [19] has presented a sector-control scheme for self-commutated half-controlled bridge converter. With this scheme, it is possible to get fundamental line power factor either at unity or leading. Krishnamurthy et al.[20,31] have suggested selective harmonic elimination technique for elimination of one or more line harmonics at a time, while maintaining fundamental power factor at unity.

1.2.2 Control of ac Controllers

The thyristor ac controllers, because of their high efficiency and compact size, are widely used in industry and domestic applications for control of ac motors and heating appliances such as furnaces, ovens, space heating etc. Power in the resistive load may be controlled by three methods, viz., phase

control, integral cycle control and forced commutation. As said earlier, the phase control method, though simple and commonly followed, has the drawback of poor line power factor and generation of high amplitudes lower order harmonics. Load voltage may be controlled continuously over a wide range with good line power factor and low line harmonics by sequence control of transformer taps incorporating line commutated thyristor-switches [23]. Integral cycle control has been described well in the literature [24-27]. In this, the load power is controlled by keeping the thyristor-switch on for an integer number of cycles out of some fixed number of cycles. This method has the outstanding property of minimizing the electromagnetic interference because the switching occurs during the natural current zero crossing. However, this method has the disadvantage of generation of sub-harmonic currents[24-27] which are more difficult to filter and may adversely affect the generator dynamics.

With forced commutation, thyristors can be turned off at any desired instant, therefore, the line conditions may be improved to a greater extent. By controlling the firing angle α and the extinction angle β, the fundamental power factor can be adjusted between leading and logging values [28]. Bland [29] has investigated such a scheme for the elimination of any one undesirable line current harmonic in a resistive load. This involves nonlinear relation between α and β, and

therefore, the implementation of such a scheme is complicated. Krishnamurthy et al. [30-31] have presented a scheme of eliminating one or more chosen line current harmonics and a scheme of reducing any one line current harmonic. In these schemes, pulses are located at fixed positions and the voltage to the resistive load is controlled by varying the pulse widths around the pulse positions. Hence the implementation of the control schemes is fairly simple.

1.3 STATIC REACTIVE POWER COMPENSATORS

The disadvantages of operating a system at low power factors, both leading as well as lagging, are well known. The major among them are poor system efficiency, poor voltage regulation and reduction in the system power transfer capacity. System stability and efficiency in a large complex power system network may be improved greatly by dynamic compensation of system Var. For obvious reasons, the conventionally used mechanically switched power capacitors cannot cope up with this requirement. Though the synchronous condensers with fast excitation response can provide the dynamic compensation to some extent, their uses are limited due to the large maintenance cost, dynamic instability, and because it is uneconomical to distribute them over the length of transmission line to maintain better voltage profile. And, this has led to the development of static VAR compensator (SVC). Because of their compact size, they can

be placed right at the load terminals for compensating individual loads like large thyristor converters in the rolling mills, arc furnaces etc. This feature has been used beneficially for transmission line voltage control over a long line by placing the compensators at discrete places along the line.

The operation and the field of application of different SVCs, comprising thyristor-switched capacitors, thyristor-controlled reactors and their combinations, have been described in several publications[32-37]. However,realisation of their control has not been emphasised in the literature. Like other thyristor controlled systems, SVC also introduces harmonics in the line current due to discontinuous current in the thyristor-controlled reactor. Normally the harmonics are filtered using external filters. Compensator cost may be reduced considerably if with suitable control the harmonics can be reduced within the compensator itself.

1.4 SCOPE AND OBJECTIVES OF THE THESIS

From the literature survey, the following points may be noted :

1) Several methods,based on line and forced commutation, have been reported for power factor improvement and harmonic reduction in ac-dc converters and ac controllers. However, no systematic comparative studies have been performed to

bring out the relative merits of one method over the other with regard to their performance measures.

2) Controlled flywheeling technique has not been considered for optimisation of reactive power in sequence control of ac-dc converters.

3) Selective harmonic elimination methods for ac-dc converter and ac controller, which are simple to realise, have been reported employing even number of pulses per half cycle of the output voltage. There is a scope to extend these methods to odd number of pulses per half cycle.

4) Many papers have been reported explaining principles and applications of static VAR compensators in power system networks. However, the details of the control schemes have not been reported so far.

5) No work has been reported for reducing the harmonics generated by the thyristor controlled reactors in static VAR compensators.

The objectives of the work reported in the thesis are :

1) To carry out the detailed comparative studies of control schemes of ac-dc converters and ac controllers.

2) To develop a method for minimising the reactive power employing controlled flywheeling to sequence control of ac-dc converters.

3) To develop methods for selective harmonic elimination in ac-dc converter and ac-controller with particular emphasis on simplicity of realisation.

4) To develop control schemes for static VAR compensators used for power factor improvement in industrial applications.

5) To develop a method for reducing the harmonics in static VAR compensator.

1.5 OUTLINE OF THE THESIS

The chapterwise summary of the thesis is given below :

Chapter 2 presents a detailed comparative study of control schemes for line- and forced-commutated single-phase ac-dc converters. Study is restricted for a maximum of two stage converters and two forced-commutations per half cycle. Assuming constant load current and ideal commutation, the comparison is made for system power factor, fundamental power factor (displacement factor), distortion factor, fundamental reactive power, line current harmonics and load current ripple. In addition, symmetrical pulse width modulation (SPWM) and asymmetrical PWM control schemes are compared for a dc series motor load. Influence of number of pulses per half cycle on the system performance has also been investigated.

Chapter 3 describes a modified sequence control for series connected line commutated single-phase bridge converters. Bridges are operated in sequence with half-controlled characteristic. A

generalised method for selecting the bridge ratings and two sequence control techniques for minimisation of reactive power over the range of control, have been described. The proposed sequence control techniques for two stage control are compared with the other five methods, viz., conventional phase-control of single bridge and two bridges in sequence, sequence control scheme of Ref. [8] and controlled flywheeling of single bridge and two bridges in sequence.

Following proper pulse width modulation control in forced-commutated converter, power factor and line current waveform can be maintained better than that in line-commutated converter. In Chapter 4, a modulation scheme is proposed for elimination of one or M unwanted line current harmonics in ac-dc converter system. Modulation scheme is characterized by equal pulse widths of fixed locations, and that simplifies its realisation. Further, it has been shown that out of the two choices, viz., modulation consisting of odd and even number of pulses per half cycle, the former one results in better performance. A control circuit for self starting the converter is developed and the feasibility of the scheme is verified experimentally.

Chapter 5 presents a comparative evaluation of different control schemes for single-phase ac controllers considering resistive load. In the case of forced-commutated controllers, the study is restricted to a maximum of two forced commutations

per half cycle. Comparison is carried out on the basis of line current harmonics, distortion factor, fundamental power factor and total power factor.

Chapter 6 deals with the performance improvement in forced-commutated ac controllers. Two improved control schemes are proposed. The first one deals with elimination of two or more number of line harmonics. Realisation of the control scheme is simple due to equal pulse widths with fixed pulse positions modulation control. A generalised algorithm for fixing the pulse positions is derived. Comparative evaluation of modulations employing odd and even number of pulses per half cycle is carried out. Suitable power circuit and control circuit for implementation of the scheme are developed. Second method deals with reduction of any one unwanted harmonic employing three pulses per half cycle. In this scheme also, like the first scheme, the modulated pulses are of equal widths and placed at appropriate locations over the half cycle.

Chapter 7 is devoted to static VAR compensators for external compensation of load reactive power. A control scheme for thyristor switched capacitor compensator for compensating the inductive loads is developed. The capacitor switching transients are eliminated by switching the thyristor-switch module at the instant when the capacitor voltage is equal to the line voltage. The scheme has been verified experimentally. Also,a

control scheme for fixed capacitor thyristor-controlled reactor compensator is presented for smooth control of reactive power. Look-up table approach is followed to simplify the control circuit realisation. Experimental results are presented. Further, two methods of reducing the line current harmonics due to TCR are described. In this the reactor current is controlled by control of transformer tap and thyristor firing angle. The feasibility of the methods are verified experimentally.

A brief review of the major contributions of this thesis and possibilities for further work are given in the concluding chapter.

CHAPTER 2

COMPARATIVE EVALUATION OF AC-DC CONVERTER CONTROL SCHEMES

2.1 INTRODUCTION

In industries and ac traction systems, ac-dc thyristor converters are extensively used for speed control of dc motors. Applications requiring motoring and regenerative control of DC machines employ fully controlled thyristor converters. The problems with the fully controlled converters operated with the conventional phase-control are the poor line power factor, generation of high magnitudes of lower order line current harmonics and large ripple in the output voltage. Several methods based on line and forced commutation for harmonic reduction and power factor improvement in converters have been reported in the literature [5 -20].

In this chapter, a detailed comparative study of some prominent control schemes for single-phase converters has been carried out. It is assumed that the load current is perfect dc and the commutation is ideal. The performance comparison is carried out on the basis of the following performance criteria :

(i) Performance on the supply side : Power factor, displacement factor, fundamental reactive power, rms line current and lower order line current harmonics.

(ii) Performance at the load side : Load current ripple and output voltage harmonics.

In the later part of this chapter, the performance of dc series motor has been evaluated for two different control schemes, viz., symmetrical pulse-width modulation (SPWM) and asymmetrical pulse-width modulation (APWM). In this study actual current waveform has been considered. Comparison is made on the basis of the performance criteria such as armature current ripple, peak armature current, harmonic content and line power factor. The influence of number of pulses per half cycle on the motor performance has also been investigated.

2.2 AC-DC CONVERTER CONTROL SCHEMES

For meaningful comparison, the present study is restricted to maximum two force commutations per half cycle of the supply voltage and two-stage sequence control. Fig. 2.1 shows the basic converter circuits for single-stage and two stage control. The commutation circuits for forced commutation operation are not shown in these figures. The details of the commutation circuit are given in Chapter 4. Fig. 2.2 shows the output voltage and line current waveforms when the single-stage and two stage converters are controlled with the schemes given below.

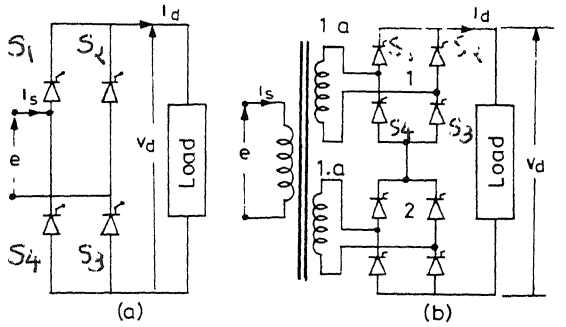


Fig.2.1 Bridge configuration. (*a*) Single stage control (*b*) Two stage control.

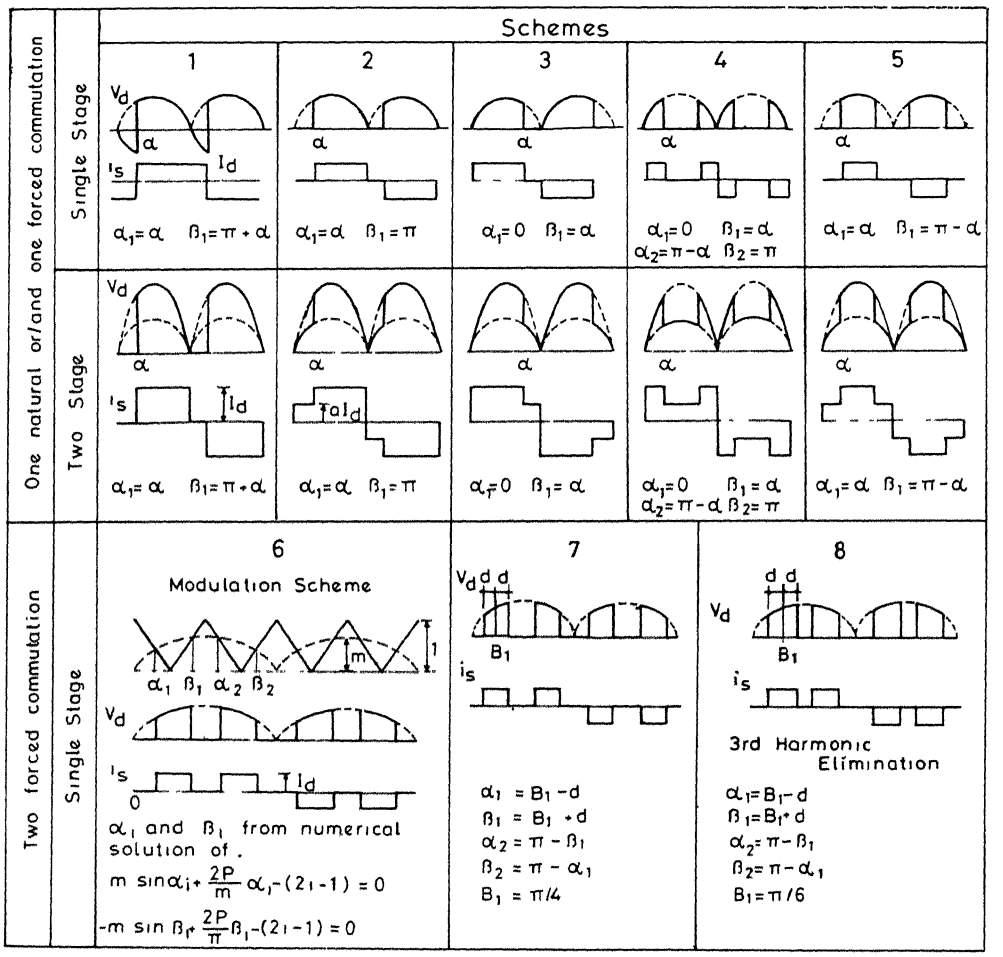


Fig.2.2 Output voltage and input current waveforms.

The numerals in the figure correspond to the order of the schemes.

(a) Single stage control with one natural commutation or/and one forced commutation per half cycle :

1. Conventional phase control [5]

In the positive half cycle when the line 'a' goes positive, thyristors S_1 and S_2 are triggered at angle α_1. In the negative half cycle S_3 and S_4 are triggered at α_1. Fig. 2.2 shows the resulting waveforms.

2. Controlled flywheeling [11]

In this, the negative excursion of voltage during rectification and positive excursion of voltage during regeneration are eliminated from the output voltage by operating the converter into controlled flywheeling mode. This permits the fully controlled converter to operate with half-controlled characteristics maintaining its regenerative capability. For rectification, the negative excursions of the output voltage are eliminated by freewheeling the load current through the thyristor pairs S_1,S_4 and S_2,S_3 by triggering the pairs at the start of the positive and negative supply half cycles respectively while the output voltage is controlled by varying the firing angle α of the pairs S_1,S_3 and S_2,S_4. Fig. 2.2 shows the resulting waveforms. Similarly, in the inversion, the positive excursions from the output voltage are eliminated by triggering the

pairs S_1,S_3 and S_2,S_4 just before the end of the positive and negative supply half cycles respectively. The output voltage is controlled by triggering the pairs S_1,S_4 and S_2,S_3 in the positive and negative half cycles respectively at the controlled angle α at which the freewheeling of the load current is initiated.

3. Extinction angle control

In the positive half cycle, S_1 and S_3 are triggered at $\omega t = 0$ to deliver the load voltage. S_1 is forced-commutated off by triggering S_2 at $\omega t = \alpha$. Now the load current freewheels through S_2 and S_3. In the negative half cycle S_2,S_3 and S_4 operate similarly.

4. Extinction angle control with two pulses per half cycle

Output voltage consists of two symmetrically located pulses per half cycle. In the positive half cycle, S_1 and S_3 are triggered at $\omega t = 0$. At $\omega t = \alpha$. S_2 is turned on which commutates S_1 and the load current freewheels through S_2 and S_3. S_1 is retriggered at $\omega t = \pi-\alpha$, which turns off S_2 and connects the load to the supply. In the negative half-cycle, S_2 and S_4 are turned on at $\omega t = 0$, which make S_1 and S_3 off. Fig. 2.2 shows the resulting waveforms.

5. Single pulse symmetrical pulse width modulation (SPWM) [13]

In the positive half-cycle when the terminal 'a' becomes

positive with respect to terminal 'b', the load current freewheels through S_1 and S_4 until S_3 is triggered. At $\omega t = \alpha$; S_3 is triggered which turns off S_4 and connects the load to the supply through S_1 and S_3. On triggering of S_2 at $\pi-\alpha$, S_1 becomes off and the load current freewheels through S_2 and S_3 until S_4 is triggered in the negative half cycle. Fig. 2.2 under numeral 5 shows the resulting waveforms.

(b) Single stage control with two forced commutations per half cycle:

6. Sinusoidal modulation with two pulses per half cycle.

Modulation technique and the resulting load voltage and line current waveforms are shown in Fig. 2.2. The triangular wave has constant amplitude and synchronised with the supply voltage. Power through the load is controlled by controlling the amplitude m of the synchronising voltage which is derived from the mains. For the ith pulse, at the intersecting points of the two waves, the following equations may be written for the turn-on angle α_i and turn-off angle β_i :

$$m\sin\alpha_i + \frac{2P}{\pi}\alpha_i - (2i-1) = 0$$

$$-m\sin\beta_i + \frac{2P}{\pi}\beta_i - (2i-1) = 0$$

α_i and β_i can be obtained from the numerical solutions of the above equations.

7. Two-Pulse SPWM

Two pulses are located symmetrically at 45^{o} and 135^{o} from the zero crossing of the supply wave. The basic principle of operation is similar to that of Scheme 5.

8. Selective harmonic elimination [20]

In this scheme the two pulses per half cycle are located at 30^{o} and 150^{o} for third harmonic elimination from the line current. The converter output voltage and the line current waveforms are given in Fig. 2.2.

(c) Two stage control

Here, the schemes 1 to 5, stated above, are considered for sequence control of two series connected bridges shown in Fig. 2.1(b). For output voltage less than 0.5 p.u., bridge 2 is operated as described in the Schemes 1 to 5 while bridge 1 freewheels the load current either through the pair S_1,S_4 or S_2,S_3. For voltage greater than 0.5 p.u., bridge 2 is kept in full conduction, i.e., thyristor pairs S_1,S_3 and S_2,S_4 are triggered alternatively at the start of each supply half cycle, while bridge 1 is controlled as described above. Output voltage and line current waveforms for voltage above 0.5 p.u. are shown in Fig. 2.2.

2.2.1 Performance Criteria

Figs. 2.3(a) and (b) shows the output voltage and the input current waveforms of two stage converter when bridge 2 is in full conduction as rectifier and bridge 1 is under control. Assuming constant load current, the performance equations for a general case of P pulse modulation scheme are given below. The values of turn on and turn off angles in Fig. 2.3 for different control schemes are given in Fig. 2.2.

(a) Output performance

(i) Output voltage harmonics

Let v_{d1} and v_{d2} be the output voltages of bridge 1 and bridge 2. Then the total output voltage

$$v_d = v_{d1} + v_{d2} \tag{2.1}$$

where $$v_{d1} = aE_m \sin\omega t \qquad \alpha_i < \omega t < \beta_i \tag{2.2}$$

$$v_{d2} = aK E_m \sin\omega t \qquad 0 < \omega t < \pi \tag{2.3}$$

and, a and K have the following values.

Single stage control : $a = 1, \quad K = 0$ (2.4)

Two stage control : $a = 0.5$ (2.5)

$K = 0 \quad 0 < r < 0.5$ (2.5)

$K = 1 \quad 0.5 < r < 1$

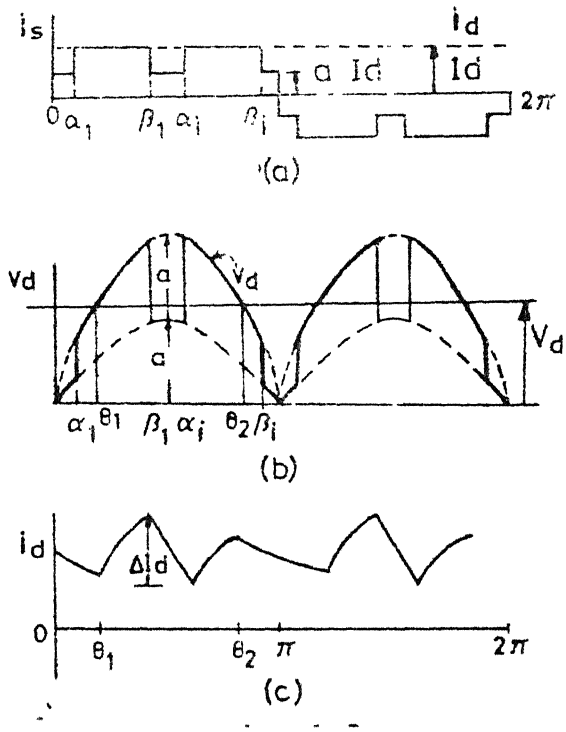


Fig. 2.3 Typical waveforms for two-stage converter
(a) Supply current with constant load current
(b) Output voltage waveform
(c) Ripple in load current

where output voltage ratio, r =

$$\frac{\text{average dc terminal voltage}}{\text{maximum average dc terminal voltage}} \qquad (2.6)$$

As $v_d(\omega t) = v_d(\omega t \pm \pi)$, only even harmonics will be present in the output voltage. From the Fourier analysis of v_d, the harmonic coefficients are given by :

$$a_o/V_{do} = v_d/V_{do} = r$$

$$= aK + a \sum_{i=1}^{P} (\cos\alpha_i - \cos\beta_i)/2 \qquad (2.7)$$

$$a_n/V_{do} = \frac{a}{2} \left[\sum_{i=1}^{P} \left(\frac{\cos N_1\alpha_i - \cos N_1\beta_i}{N_1} - \frac{\cos N_2\alpha_i - \cos N_2\beta_i}{N_2} \right) - \frac{4K}{N_1 N_2} \right] \qquad (2.8)$$

$$b_n/V_{do} = \frac{a}{2} \sum_{i=1}^{P} \left(\frac{\sin N_1\alpha_i - \sin N_1\beta_i}{N_1} - \frac{\sin N_2\alpha_i - \sin N_2\beta_i}{N_2} \right) \qquad (2.9)$$

where

V_d = average dc voltage

$V_{do} = 2E_m/\pi$

$N_1 = n+1$, $N_2 = n-1$ and $n = 2,4, \ldots$

From eqns. (2.8) and (2.9), the peak harmonic component is given by

$$V_n/V_{do} = \left[\left(\frac{a_n}{V_{do}}\right)^2 + \left(\frac{b_n}{V_{do}}\right)^2 \right]^{1/2} \qquad (2.10)$$

(ii) Voltage ripple factor

As the output voltage of the converter is not smooth and the load inductance is of finite value, the load current will

have ac ripple superimposed over the average load current. AC ripple causes additional losses in the dc machines and adversely affects the commutation. From the load consideration, the converter performance is judged from the measure of peak-to-peak of ripple in the load current. Ripple can be kept to a specified value by placing proper value of smoothing inductance in the load circuit. However, the value of the smoothing inductance depends upon the converter control scheme. Below a voltage ripple factor RF has been defined. It is a measure of inductance requirement for a specified ripple current ΔI_d or vice versa.

Neglecting the load resistance and assuming load voltage to be equal to the average output voltage V_d, the differential equation of the load current relating the smoothing inductance L is given by

$$\frac{di_d}{d\omega_t} = \frac{v_d - V_d}{2\pi f L} \qquad (2.13)$$

The typical waveforms of instantaneous load voltage v_d and load current i_d are shown in Figs. 2.3(b),(c). If θ_1 and θ_2 be the angles of the points of intersection between v_d with V_d, then, in the interval $\theta_1 < \omega t < \theta_2$, i_d will rise where $v_d > V_d$ and fall where $v_d < V_d$. From eqn. (2.13), the incremental change in the load current from the average value I_d is given by

$$i_d = \frac{V_{do}}{L \cdot f} \int_{\theta_1}^{\theta_2} \left(\frac{v_d}{V_{do}} - r\right) \frac{d\omega t}{2\pi} \qquad (2.14)$$

$$= \frac{V_{do}}{fL} R_f$$

where $R_f = \int_{\theta_1}^{\theta_2} \left(\frac{v_d}{V_{do}} - r\right) \frac{d\omega t}{2\pi}$ (2.15)

Let R_{fmax} and R_{fmin} be the maximum positive and negative values of R_f in the interval $\theta_1 < \omega t < \theta_2$. Then, from eqn. (2.14), the peak to peak ripple current is given by

$$\Delta I_d = \frac{V_{do}}{Lf} RF \qquad (2.16)$$

where voltage ripple factor, $RF = R_{fmax} - R_{fmin}$ (2.17)

Figs. 2.5(k) and 2.6(k) show the variation of RF with the output voltage ratio for the different control schemes. Eqn. (2.16) reveals that for a specified ripple ΔI_d, the smoothing inductance and voltage ripple factor are linearly related. Thus Figs. 2.5(k) and 2.6(k) directly give the comparative picture of smoothing inductance requirement in different schemes for a specified ripple current. The scheme having lower RF is better from the load consideration.

b. Input performance

(i) Line current harmonics

Let i_{s_1} and i_{s_2} be the line currents due to bridge 1 and bridge 2. Then, the total line current

$$i_s = i_{s_1} + i_{s_2} \tag{2.18}$$

where $i_{s_1} = aI_d, \quad \alpha_i < \omega t < \beta_i$ (2.19)

$$i_{s_2} = aKI_d, \quad 0 < \omega t < \pi$$

As $i_s(\omega t) = -i_s(\omega t+\pi)$, only odd harmonics are present in the line current. From eqns. (2.18) and (2.19), the harmonics components are given by

$$a_n/I_d = \frac{2a}{\pi n} \left[\sum_{i=1,P} (\sin n\beta_i - \sin n\alpha_i) \right] \tag{2.20}$$

and

$$b_n/I_d = \frac{2a}{\pi n} \left[\sum_{i=1,P} (\cos n\alpha_i - \cos n\beta_i) + 2K \right] \tag{2.21}$$

The rms value of harmonic current is given by

$$I_n/I_d = [(a_n/I_d)^2 + (b_n/I_d)^2]^{1/2}/\sqrt{2} \tag{2.22}$$

(ii) rms line current

From eqn. (2.22), rms line current may be expressed as

$$I_{rms}/I_d = \left[\sum_{n=1,3,\ldots} (I_n/I_d)^2 \right]^{1/2} \tag{2.23}$$

(iii) Fundamental power factor [5]

From eqns. (2.20) and (2.21) the fundamental power factor (displacement factor) FPF is given by

$$FPF = \cos \tan^{-1}(a_1/b_1) \tag{2.24}$$

(iv) Distortion factor

Distortion factor DF is defined as the ratio of the fundamental line current to the rms line current, i.e.,

$$DF = I_1/I_{rms} \tag{2.25}$$

(v) Total power factor (P.f)

$$\text{Total power} = E_{rms}.I_{rms}.Pf = E_{rms}.I_1.FPF$$

$$\text{Hence} \quad P.f = FPF.I_1/I_{rms}$$

$$= FPF.DF \tag{2.26}$$

(vi) Fundamental reactive power

Reactive power will be produced when only the line current waveform is asymmetrical with respect to the source voltage. In the sequence control scheme, the converters which are in freewheeling mode or in full conduction - either in inversion or rectification - do not consume reactive power. Hence, from eqns. (3.4) and (3.5) of Chapter 3, the reactive power generated by a bridge converter with conventional control and with controlled flywheeling are given as follows :

Controlled flywheeling :

$$q = [r_i(a-r_i)]^{1/2} \tag{2.27}$$

where r_i = output voltage of converter under control

$$= \frac{a}{2}(1+\cos\alpha)$$

Conventional control :

$$q = (a^2 - r_i^2)^{1/2} \qquad (2.28)$$

where

$$r_i = a\cos\alpha$$

Figs. 2.5(i) and 2.6(i) show the variation of reactive power for the schemes 1 to 3.

2.2.2 Comparative Performance

The comparative performance has been presented in Figs. 2.4 - 2.6. The following can be noted from these figures.

2.2.2.1 Supply current harmonics

(a) Single stage control

(1) Harmonic content in conventional fully-controlled operation does not vary with the output voltage ratio while it varies in case of other schemes.

(2) Peak values of harmonics in schemes 2,3 and 5 are equal to their constant values under fully controlled operation.

(3) Filter size is decided by lowest order harmonics. Hence, in this respect scheme 8 is the best followed by 6. Scheme 7 is no way better than 1,2 and 3. Scheme 4 is the worst.

(b) Two stage control

(4) Harmonic contents are reduced to half of that in single stage for the voltage ratio less than 0.5, but no change for voltage ratio > 0.5.

2.2.2.2 Output voltage harmonics

(a) Single stage control

(5) Scheme 4 has least amount of harmonics followed by 2,3,5 and 1. Schemes 6-8 offer better performance (lower harmonics) compared to 1-5.

(b) Two stage control

(6) Voltage harmonics are reduced, particularly at low output voltages.

(7) Among all the schemes 1-8, scheme 7 offers the best performance over the entire voltage range.

2.2.2.3 Load voltage (load current ripple) ripple

(8) Same as in output voltage harmonics.

2.2.2.4 Reactive power

(a) Single stage control

(9) Reactive power requirement reduces to half in half controlled operation

(10) Reactive power becomes 0 in schemes 4-8 and it is leading in 3.

(b) Two stage control

(11) Two stage control reduces the reactive power further; schemes 2 and 3 in two stage control have peak reactive power one fourth that of conventional control.

2.2.2.5 Fundamental PF

(12) Lagging for schemes 1 and 2, leading for 3 and unity for 4-8.

2.2.2.6 Distortion factor

Distortion factor is a measure of total harmonic content in supply current. The higher the distortion factor, the lower the harmonic content.

(a) Single stage control

(13) Lowest harmonic content in scheme 1 followed by 2 and 3,5,8,6,7 and 4.

(b) Two stage control

(14) Higher values of distortion factor are obtained with two stage control. For voltage ratio < 0.5 schemes 2 and 3 offer maximum distortion factor followed by 1,5 and 4. For voltage ratio > 0.5, 1 and 5 have highest distortion factor followed by 2 and 3, and 4.

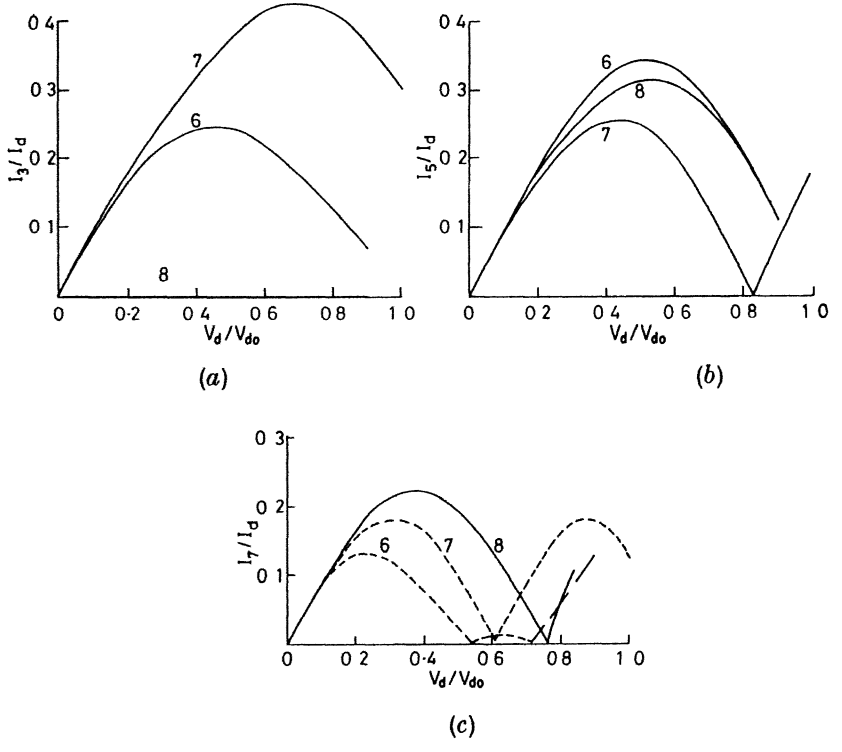


Fig.2.4 Supply current harmonics in single stage converter with two forced commutations/half cycle. (*a*) third harmonic. (*b*) fifth harmonic. (*c*) seventh harmonic.

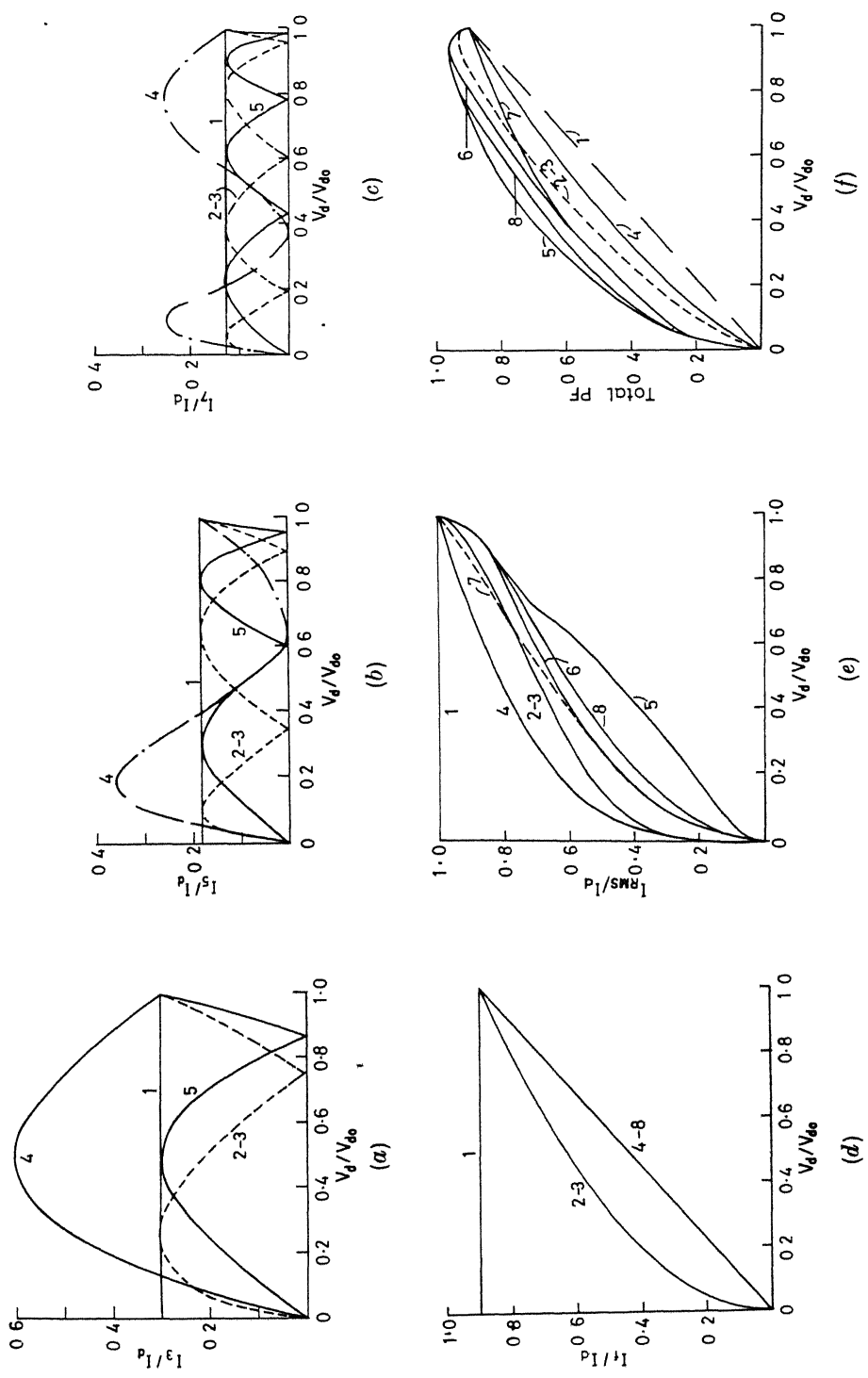


Fig. 2.5 (contd...)

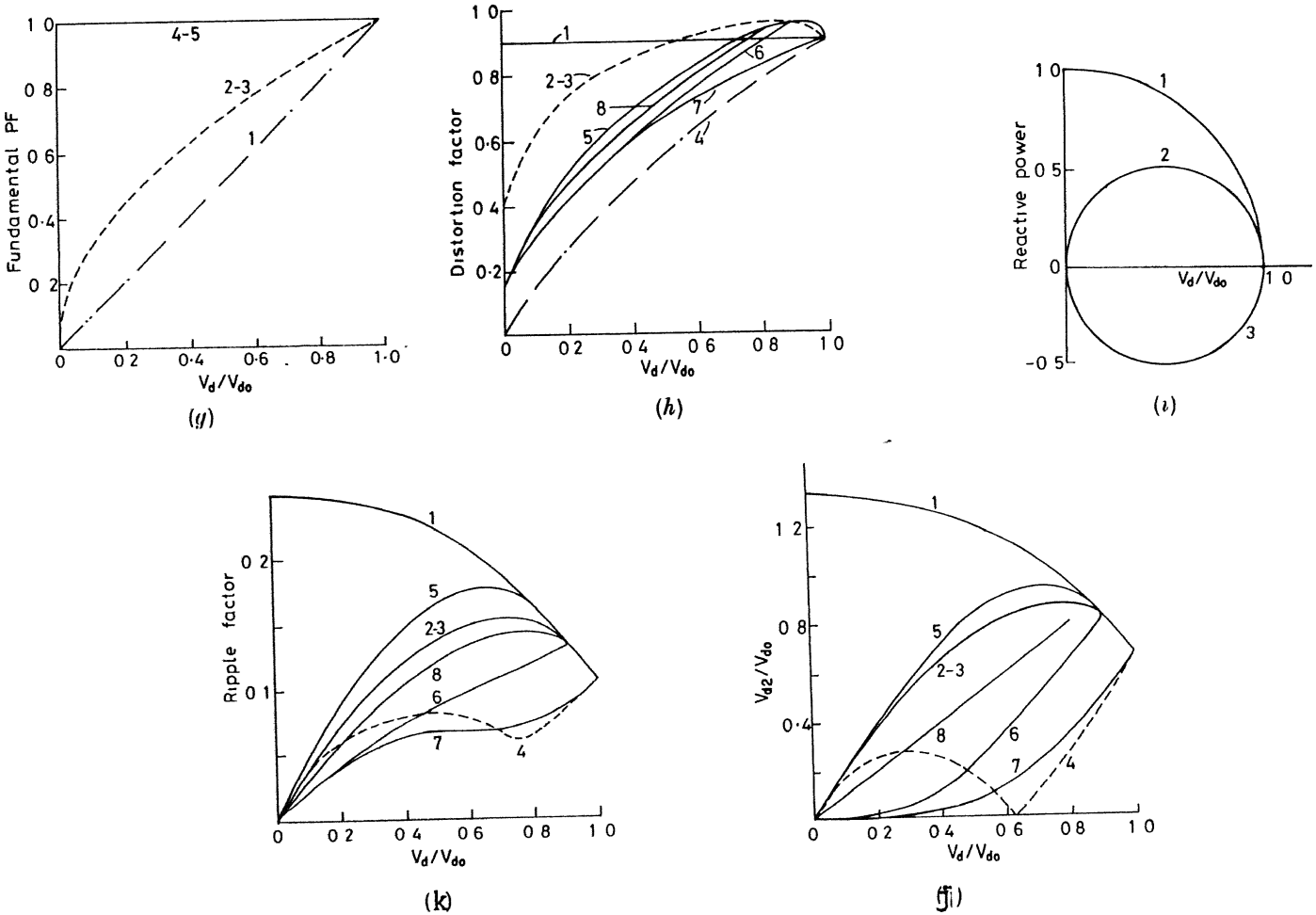


Fig.2.5 Single stage converter control. (*a*) third harmonic current. (*b*) fifth harmonic current (*c*) seventh harmonic current, (*d*) Fundamental supply current. (*e*) RMS supply current. (*f*) Total power factor. (*g*) Fundamental power factor. (*h*) Distortion factor. (*i*) Reactive power locus. (*j*) second harmonic output voltage. (*k*) Voltage ripple factor.

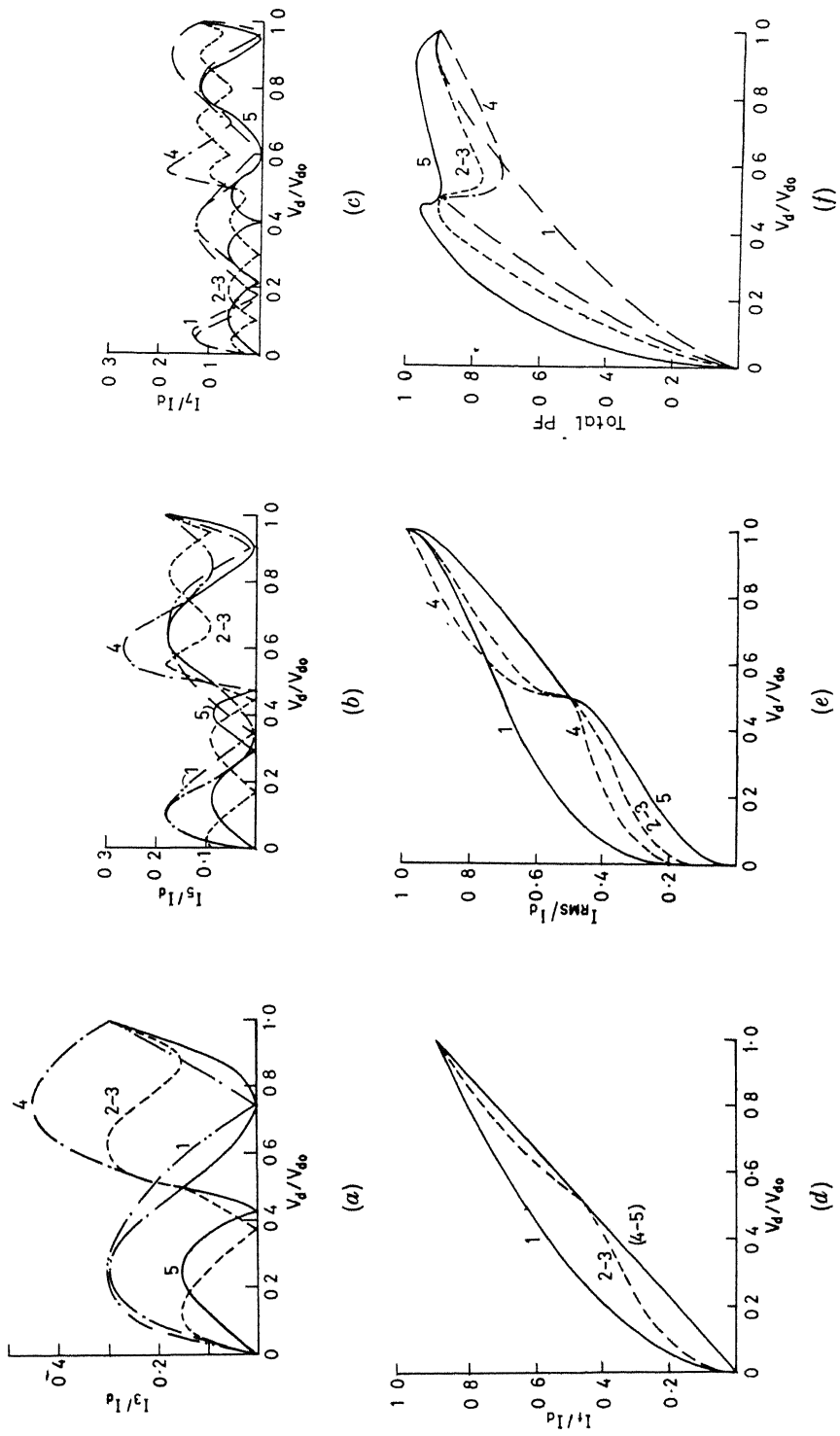


Fig. 2.6 (contd ...)

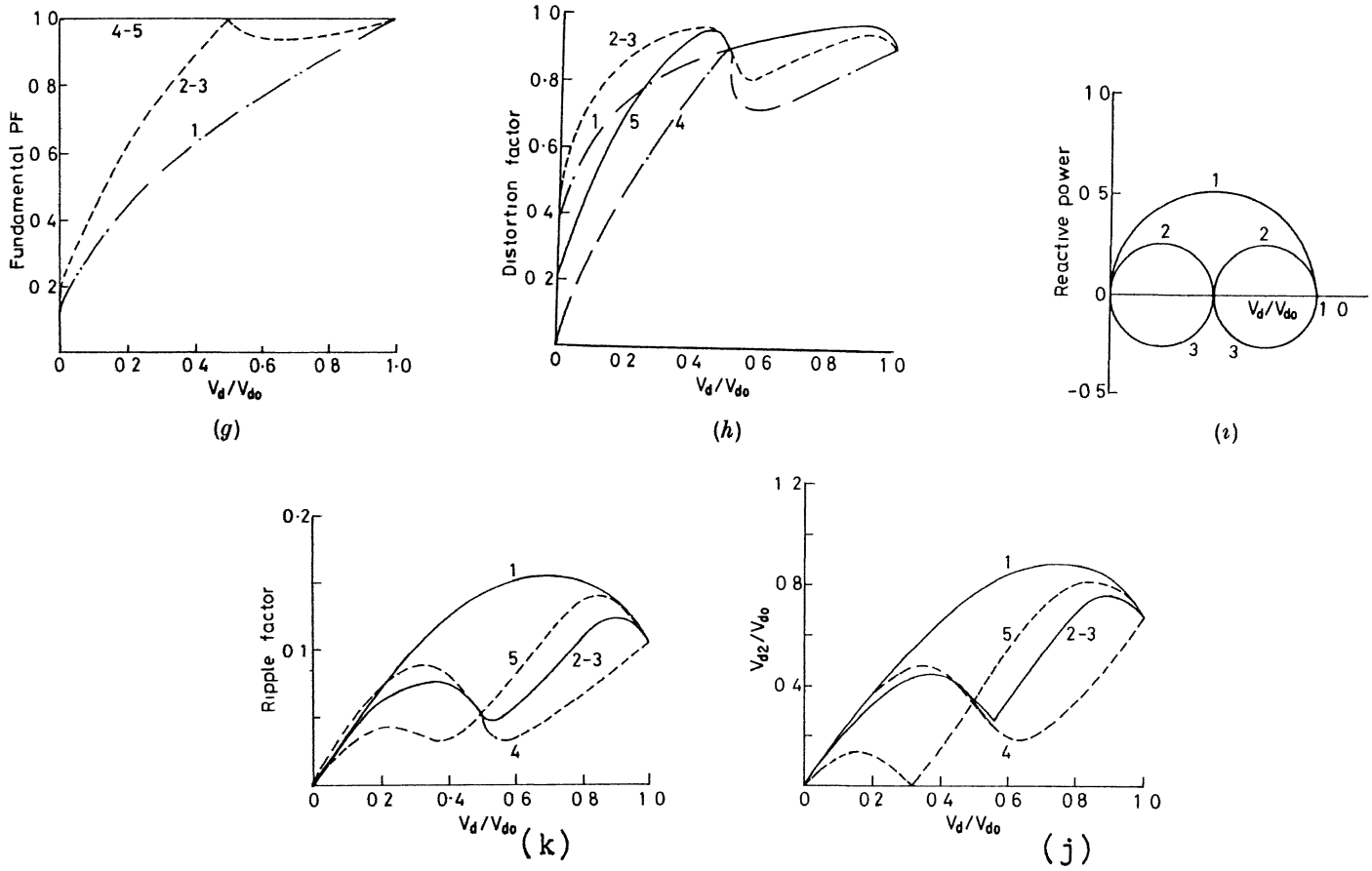


Fig. 2.6 Two stage converter control. (*a*) third harmonic current. (*b*) fifth harmonic current. (*c*) seventh harmonic current. (*d*) Fundamental supply current. (*e*) RMS supply current. (*f*) Total power factor. (*g*) Fundamental power factor (*h*) Distortion factor. (*i*) Reactive power locus. (*j*) second harmonic output voltage (*k*) Voltage ripple factor.

2.2.2.7 Total Power Factor

(a) Single stage control

(15) Scheme 5 gives the highestp.f followed by 8,6,7,2 and 3,4 and 1.

(b) Two stage control

(16) p.f.is further improved with two stage control. The scheme 5 provides the bestp.f.followed by 2 and 3,4 and 1.

2.3 SYMMETRICAL AND ASYMMETRICAL PULSE WIDTH MODULATION CONTROL FOR DC SERIES MOTOR

In Ref. [15], drive performance has been investigated employing APWM control for maximum three pulses per half cycle of supply voltage. In such case, as the output waveform does not have quarterwave symmetry, the fundamental power factor of the line current will not be unity. It was therefore felt that the use of symmetrical pulses would be more appropriate. In view of this the drive performance was investigated for symmetrically as well as asymmetrically located pulses for varying number of pulses upto seven per half cycle. The comparative study of these two approaches has been presented in the following :

2.3.1 Analysis

Fig. 2.7(a) shows the voltage applied to the dc series motor by operating the converter (Fig. 2.1(a)) with general

pulse-width modulation control, comprising P pulses per supply half cycle. Figs. 2.7(b) and (c) show the resulting armature current and line current waveforms. To simplify the analysis, the following assumptions are made :

(i) Thyristors and diodes are considered as ideal switches;

(ii) Effect of commutation circuit on the load voltage waveform is negligible;

(iii) Motor parameters R_a,L_a and M_{af} remain constant;

(iv) Mechanical time constant of the motor is much larger than the pulse period and hence the motor speed remains constant during a given operating condition;

(v) Occurrence of discontinuity in the armature current under light load is over a very narrow region of torque-speed plane and hence current is assumed to be continuous; and

(vi) Residual field effect in the motor is negligible.

As the armature current is assumed to be continuous, motor exhibits two modes, viz., power mode, in which armature gets connected to the source and freewheeling mode, in which the armature current freewheels through the thyristors connected to the same line terminal. Referring to Fig. 2.7(b), in the interval $\alpha_i \leq \omega t \leq \alpha_{i+1}$, the circuit equations for different modes may be written as follows.

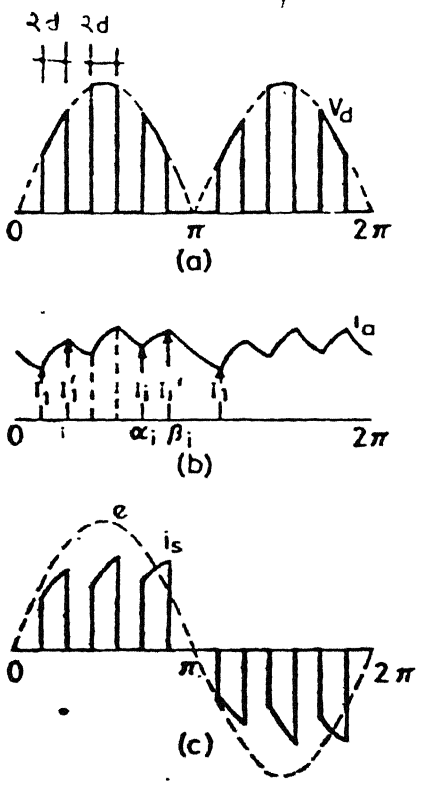


Fig. 2.7 Converter waveforms with finite inductance in the output circuit
(a) Load voltage (b) Load current
(c) Supply current

Power Mode :

$$E_m \sin\omega t = R_a i_d + L_a \frac{di_d}{dt} + M_{af}.S.i_d \qquad \alpha_i \leq \omega t \leq \beta_i \tag{2.29}$$

with initial and final conditions

$$i_d(\alpha_i) = I_i \ , \tag{2.30}$$

and $\quad i_d(\beta_i) = I_i'$

From these two equations

$$i_d = I_m[\sin(\omega t-\phi) - \sin(\alpha_i-\phi) \exp\left(\frac{\alpha_i-\omega t}{Q}\right)] + I_i \exp\left(\frac{\alpha_i-\omega t}{Q}\right) \tag{2.31}$$

where $I_m = \frac{E_m}{Z}$, $\quad Z = [R_a^2 + (\omega L_a)^2]^{1/2}$,

$\phi = \cos^{-1}\left(\frac{R_a}{Z}\right)$, and $Q = \frac{\omega L_a}{(R_a+M_{af}.S)}$

Freewheeling Mode :

$$0 = R_a i_d + L_a \frac{di_d}{dt} + M_{af}.S.i_d \qquad \beta_i \leq \omega t \leq \alpha_{i+1} \tag{2.32}$$

with the initial and final conditions

$$i_d(\beta_i) = I_i' \quad \text{and} \quad i_d(\alpha_{i+1}) = I_{i+1} \tag{2.33}$$

Therefore,

$$i_d = I_i' \exp\left(\frac{\beta_i-\omega t}{Q}\right) \tag{2.34}$$

I_i and I_i' in eqns (2.31) and (2.34) may be determined as follows :

Taking the average of eqns. (2.29) and (2.32) over the period π, we get,

$$\sum_{i=1}^{P} (\cos\alpha_i - \cos\beta_i) = D\, I_{dav} \qquad (2.35)$$

where $D = \pi(R_a + SM_{af})/E_m$,

I_{dav} = average value of armature current.

α_i and β_i are function of pulse width. In the two schemes under study, the pulse width as a function of speed S and current I_{av} may be determined as follows :

SPWM Control :

In this scheme, P pulses of equal widths are placed over a half cycle at equal distance and symmetrically about $\pi/2$ axis. Their positions are given by

$$B_i = \frac{\pi}{2P}(2i-1), \quad i = 1 \text{ to } P \qquad (2.36)$$

The output voltage is controlled by varying the pulse widths symmetrically around the pulse positions. Therefore,

$$\alpha_i = B_i - d,$$
$$\beta_i = B_i + d \qquad (2.36)$$

Substituting eqn. (2.36) in eqn. (2.35) gives

$$d = \sin^{-1}\left(\frac{D\, I_{dav}}{2 \sum_{i=1}^{P} \sin B_i}\right) \qquad (2.37)$$

APWM Control :

In this, the leading edges of P pulses of equal widths are fixed at the positions

$$B_i = \frac{\pi}{P}(i-1), \qquad i = 1 \,..\, P \qquad (2.38)$$

and the voltage is controlled by shifting the trailing edges of the pulses. Hence,

$$\alpha_i = B_i \,, \qquad \beta_i = B_i + 2d \qquad (2.39)$$

From eqns. (2.35) and (2.39)

$$d = \frac{1}{2}\tan^{-1}\left(\frac{\sum_{i=1}^{P} \cos B_i}{\sum_{i=1}^{P} \sin B_i}\right) + \frac{1}{2}\sin^{-1}\left[\left(D\, I_{dav} - \sum_{i=1}^{P} \cos B_i\right)/A\right] \qquad (2.40)$$

where $A = \mathrm{SQRT}\left[\left(\sum_{i=1}^{P} \sin B_i\right)^2 + \left(\sum_{i=1}^{P} \cos B_i\right)^2\right]$

From eqns. (2.23) - (2.24), (2.32) - (2.34) and (2.37) or (2.40) as the case may be, I_i and I_i' can be determined by two

methods, viz., closed form expressions and iterative technique. For small value of P first approach is convenient, while for large value of P, the second one is convenient. In the present study, as P is of varying number, the second method is preferred.

2.3.2 Performance Characteristics

(a) Output characteristics

The average power and torque of the motor can be expressed as follows :

Back emf, $e_b = M_{af} \cdot S \cdot i_d$

Therefore,

motor power $P_m = \frac{1}{\pi} \int_0^{\pi} e_b \cdot i_d \, d\omega t$

$$= M_{af} \cdot S \, I_{drms}^2 \qquad (2.41)$$

As the current ripple is usually small for such a drive the rms current I_{drms} is nearly equal to the average current I_{dav} [21]. In eqn. (2.41) substituting I_{dav} for I_{drms} gives

$$P_m = M_{af} \cdot S \cdot I_{dav}^2 \qquad (2.42)$$

or

$$I_{dav} = \left(\frac{P_m}{M_{af} \cdot S}\right)^{1/2} \qquad (2.43)$$

Hence,

$$\text{Torque, } T = P_m/S = M_{af} \cdot I_{dav}^2 \qquad (2.44)$$

Due to unsmooth converter voltage, instantaneous armature current i_d fluctuates between I_{dmax} and I_{dmin} over I_{dav}. Ripple in the armature current causes commutation problem and increases the losses in the motor. Ripple factor as a measure of armature current ripple is defined as

$$RF = \frac{I_{dmax} - I_{dmin}}{I_{base}} \tag{2.45}$$

where I_{base} is taken as motor rated current. I_{dmax} and I_{dmin} may be determined from eqns. (2.31) and (2.34).

(b) Input characteristics

From Fig. 2.7(c), the line current in the positive half cycle is given as

$$i_s = i_d \qquad \alpha_i \leq \omega t \leq \beta_i \tag{2.46}$$

$$= 0 \qquad \text{elsewhere}$$

$$\text{Also, } i_s(\omega t) = -i_s(\omega t + \pi) \tag{2.47}$$

From eqns. (2.31), (2.46) and (2.47), the Fourier coefficients and rms line current for the waveform shown in Fig. 2.7(c) are derived and they are given below.

$$a_1 = A \sum_{i=1}^{P} \left[\frac{\cos(2\alpha_i - \phi) - \cos(2\beta_i - \phi)}{2-(\beta_i - \alpha_i)\sin\phi}\right] \tag{2.48}$$

$$+ B \sum_{i=1}^{P} I_i\left[\left(\sin\beta_i - \frac{\cos\beta_i}{Q}\right) \exp\left(-\frac{\beta_i}{Q}\right)\right.$$

$$\left. - \left(\sin\alpha_i - \frac{\cos\alpha_i}{Q}\right) \exp\left(-\frac{\alpha_i}{Q}\right)\right]$$

$$b_1 = A \sum_{i=1}^{P} \left[\frac{\sin(2\alpha_i-\phi) - \sin(2\beta_i-\phi)}{2+(\beta_i-\alpha_i)\cos\phi}\right] \tag{2.49}$$

$$-B \sum_{i=1}^{P} I_i\left[\left(\cos\beta_i + \frac{\sin\beta_i}{Q}\right) \exp\left(-\frac{\beta_i}{Q}\right)\right.$$

$$\left.-\left(\cos\alpha_i + \frac{\sin\alpha_i}{Q}\right) \exp\left(-\frac{\alpha_i}{Q}\right)\right]$$

$$a_n = A \sum_{i=1}^{P} \left[\frac{\cos(N\alpha_i-\phi) - \cos(N_1\beta_i-\phi)}{N_1}\right. \tag{2.50}$$

$$\left. - \frac{\cos(N_2\alpha_i+\phi) - \cos(N_2\beta_i+\phi)}{N_2}\right]$$

$$+B \sum_{i=1}^{P} I_i\left[\left(n\sin n\beta_i - \frac{\cos n\beta_i}{Q}\right) \exp\left(-\frac{\beta_i}{Q}\right)\right.$$

$$\left.-\left(n\cos n\alpha_i - \frac{\cos n\alpha_i}{Q}\right) \exp\left(-\frac{\beta_i}{Q}\right)\right]$$

$$b_n = A \sum_{i=1}^{P} \left[\frac{\sin(N_2\beta_i+\phi) - \sin(N_2\alpha_i+\phi)}{N_2}\right. \tag{2.51}$$

$$\left. - \frac{\sin(N_1\beta_i-\phi) - \sin(N_1\alpha_i-\phi)}{N_1}\right]$$

$$-B \sum_{i=1}^{P} I_i\left[\left(n\cos n\beta_i + \frac{\sin n\beta_i}{Q}\right) \exp\left(-\frac{\beta_i}{Q}\right)\right.$$

$$\left. - \left(n\cos n\alpha_i + \frac{\sin n\beta_i}{Q}\right) \exp\left(-\frac{\alpha_i}{Q}\right)\right]$$

and the rms line current,

$$I_{rms} = \left(\sum_{i=1}^{P} \int_{\alpha_i}^{\beta_i} \frac{i_s^2}{\pi} \, d\omega t \right)^{1/2}$$

$$= \sum_{i=1}^{P} \left[\pi A^2 \left(\frac{\beta_i - \alpha_i}{2} - \frac{\sin 2(\beta_i - \phi) - \sin 2(\alpha_i - \phi)}{4} \right) \right. \tag{2.52}$$

$$+ \frac{QI_i^2}{2\pi} \left(\exp\left(-\frac{2\alpha_i}{Q}\right) - \exp\left(-\frac{2\beta_i}{Q}\right) \right)$$

$$- AB\left(\left(\frac{\sin(\beta_i - \phi)}{Q} + \cos(\beta_i - \phi) \right) \exp(\beta_i / Q) \right.$$

$$\left. \left. - \left(\frac{\sin(\alpha_i - \phi)}{Q} + \cos(\alpha_i - \phi) \exp\left(-\frac{\alpha_i}{Q}\right) \right) \right) \right]$$

where $N_1 = n+1$, $N_2 = n-1$, $A = \frac{E_m}{2Z}$,

$$B = \frac{2Q^2}{\pi(1+Q^2)} \quad \text{and} \quad n = 3,5, \ldots$$

Different input performance characteristics are now given below.

Rms line current harmonic,

$$I_n = \left[\frac{a_n^2 + b_n^2}{2} \right]^{1/2} \tag{2.53}$$

Fundamental power factor,

$$FPF = \cos\left[\tan^{-1} \left(\frac{a_1}{b_1} \right) \right] \tag{2.54}$$

Total power factor,

$$p.f. = FPF. \frac{I_1}{I_{rms}} \tag{2.55}$$

where I_1 = rms fundamental line current

$$= \left(\frac{a_1^2 + b_1^2}{2}\right)^{1/2}$$

The harmonic content I_H, which indicates the harmonic distortion in the line current, is given by

$$I_H = \left(\frac{I_{rms}^2 - I_1^2}{I_1^2}\right)^{1/2} \qquad (2.56)$$

2.3.3 Computation of Performance Characteristics

For the evaluation of the relative performance of the two schemes various performance parameters are evaluated for a given power. Here comparison are done for the power levels of 0.37 p.u. and 0.75 p.u. The motor parameters are [15] R_a = 1.0 Ohms, L_a = 0.012 Ohms, M_{af} = 0.027 H, rated motor current = 17.5 amp (= 1 p.u.), E_m = 170 V and S = 183.2 rad/sec. (= 1 p.u.). The computation procedure, for the specified value of power P_m and operating speed S, is as follows :

Step 1 : Compute I_{dav} from eqn. (2.43).

Step 2 : Compute d (half pulse width) from eqn. (2.37) or (2.40) as the case may be.

Step 3 : Compute I_i and I_i' from eqns. (2.23) - (2.24) and (2.32) - (2.34) by iterative technique.

Step 4 : Once I_i and I_i' are known, the different performance characteristics can be computed.

Figs. 2. 8 - 2.13 show the variation of the different performance characteristics with the speed in the two schemes involving 1,3 and 5 pulses per half cycle.

2.3.4 Comparative Evaluation of Control Schemes

Figs. 2.8 to 2.13 depict the comparative performance of SPWM and APWM schemes. From these figures it could be seen that the two schemes differ in performance only for the case of single pulse per half cycle while for higher number of pulses, i.e., 3 and above, both the schemes have almost similar performance.

For the schemes with single pulse modulation following comparison may be made :

(i) The fundamental power factor for SPWM scheme remains very near to unity value for any speed and power, whereas in APWM scheme the power factor, which is leading, is low at low speeds and increases with increased speed and power.

(ii) At low speeds, SPWM has higher power factor, and at higher speeds both the schemes have almost same power factor.

(iii) At low power, the third harmonic current and harmonic content in SPWM are higher, which reduce with the increase of motor power. At higher power levels both the schemes have nearly the similar performance.

(iv) Ripple content in SPWM scheme is higher.

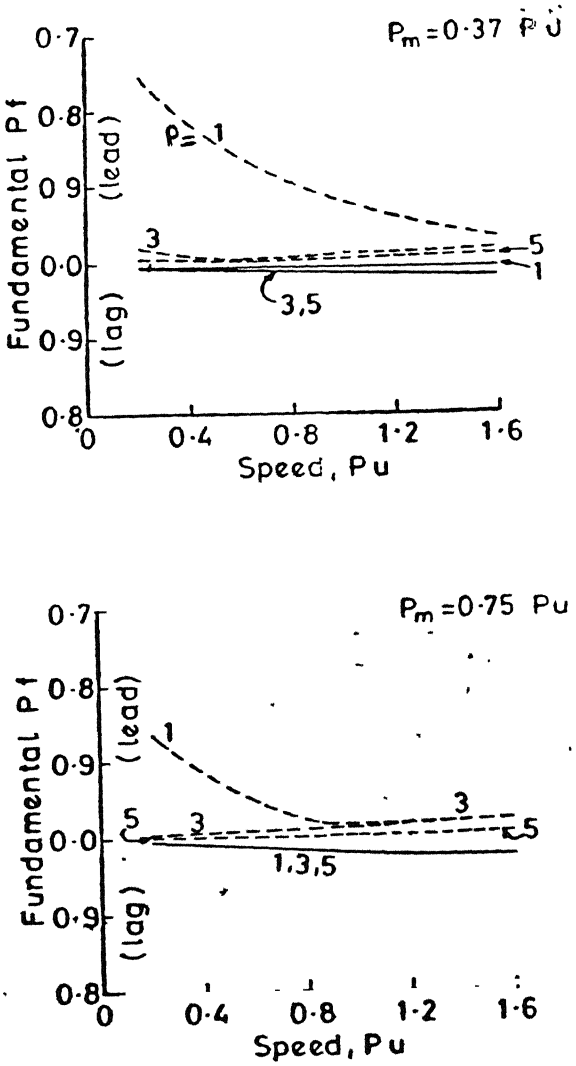


Fig.2.8 Fundamental power factor variation (numerals indicate the pulses/half cycle)

SPWM

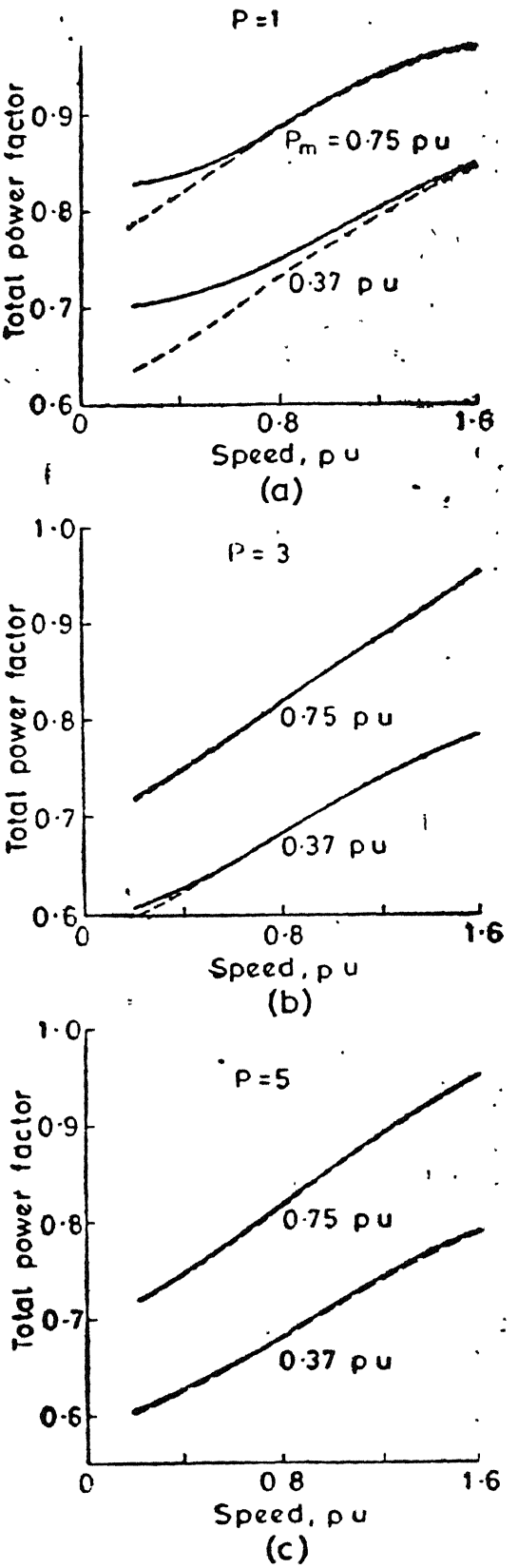


Fig. 2.9 Total power factor variation

——— SPWM
---- APWM

Acc. No. A 99161

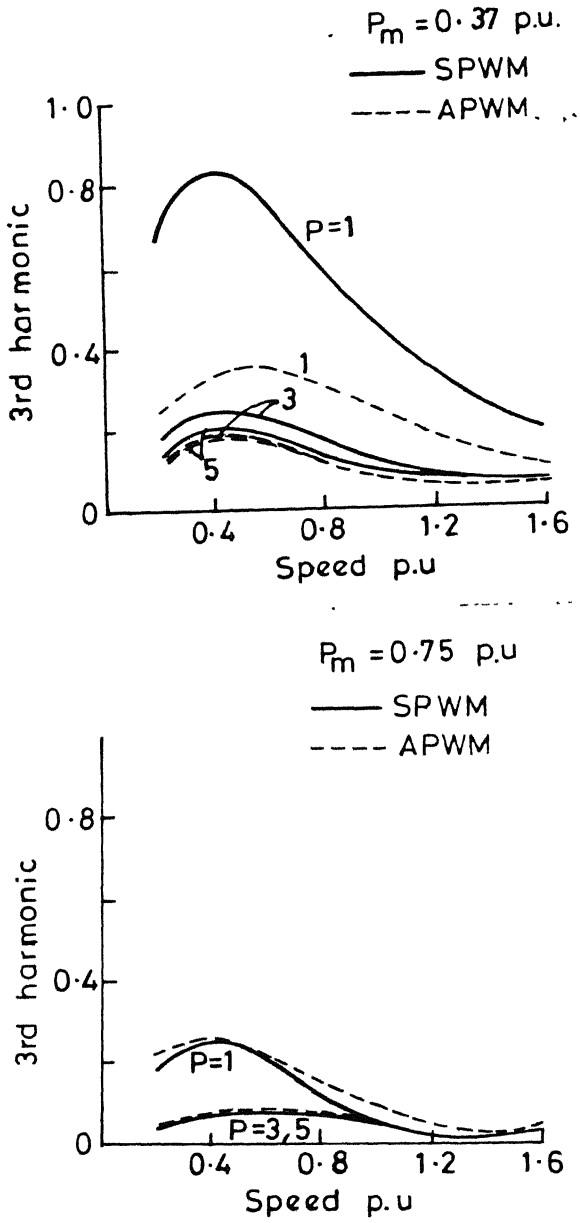


Fig.2.10 Third harmonic variation

SPWM
APWM

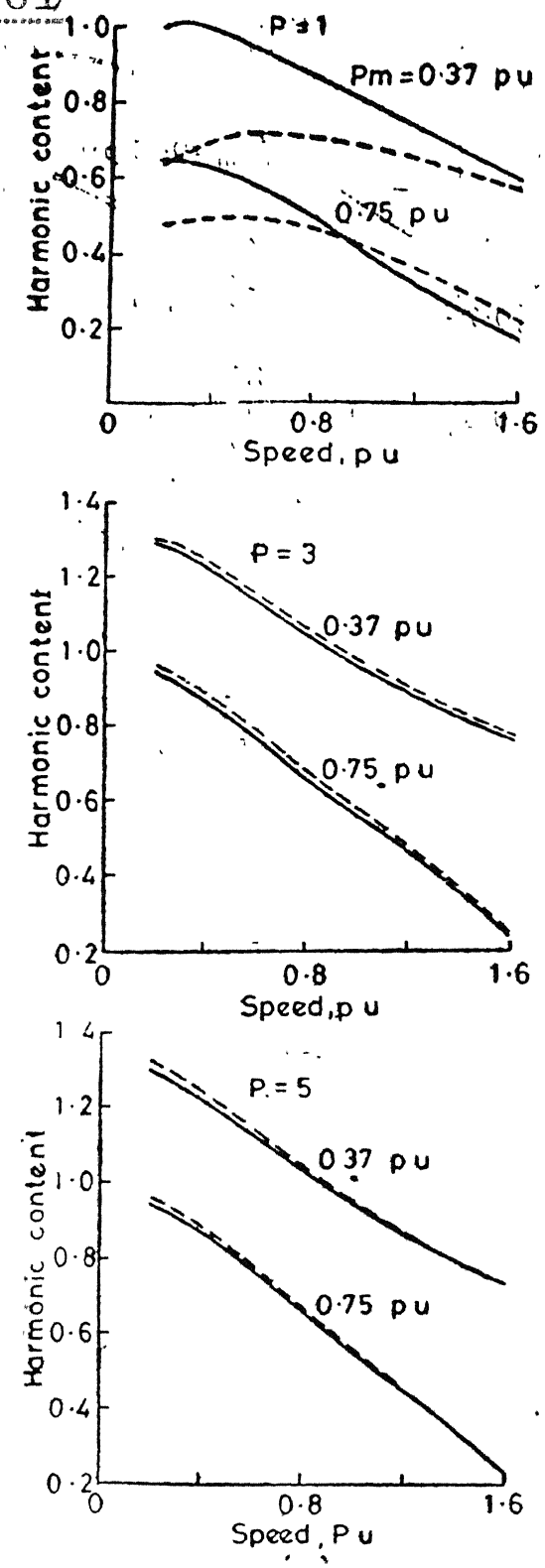


Fig.2.11 Harmonic content variation

SPWM
APWM

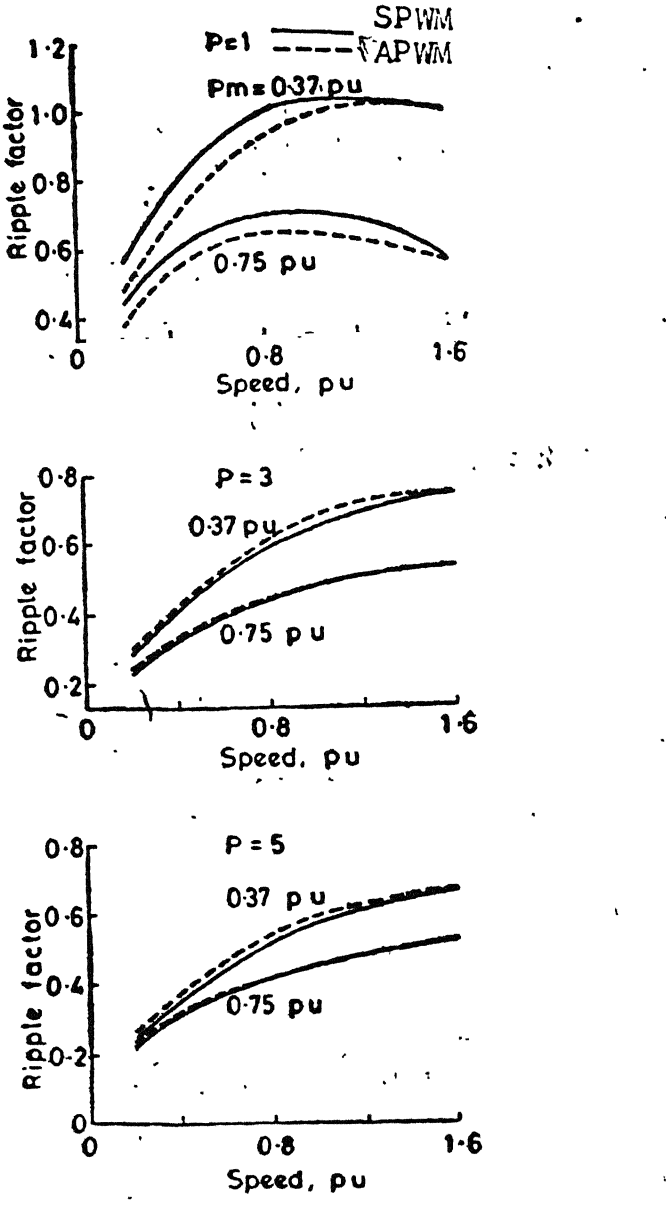


Fig.2.12 Ripple factor variation

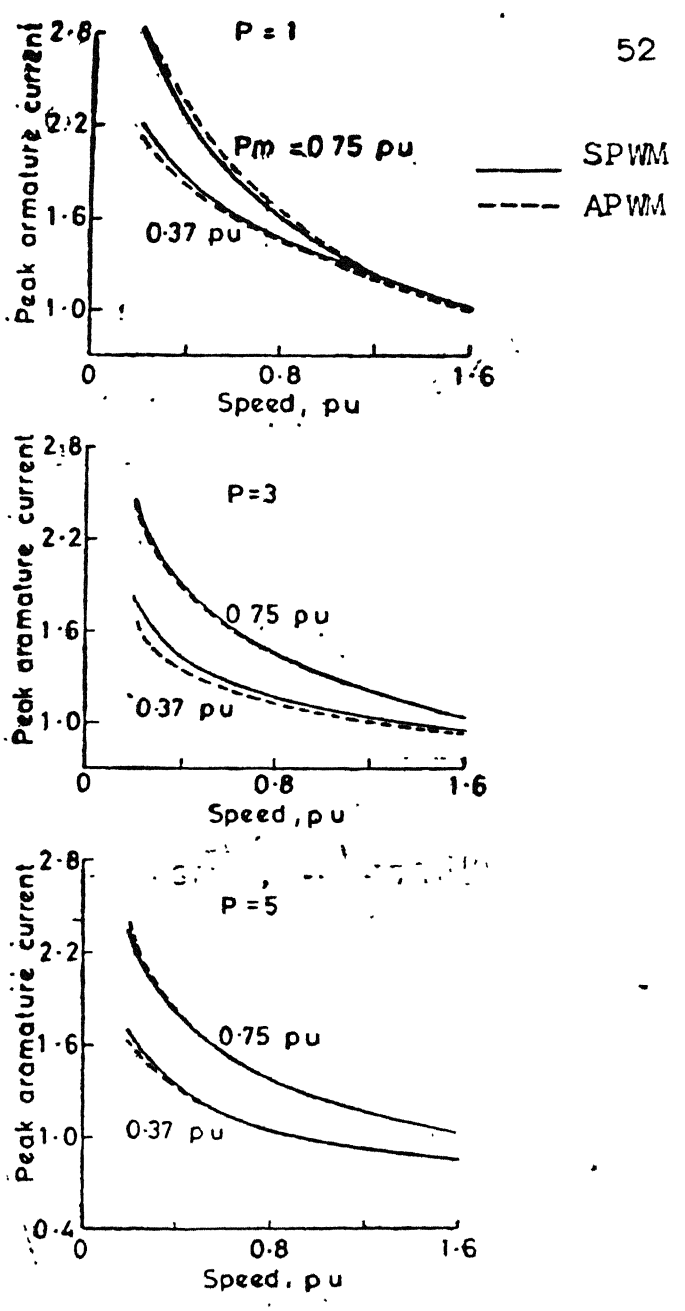


Fig.2.13 Peak armature current variation

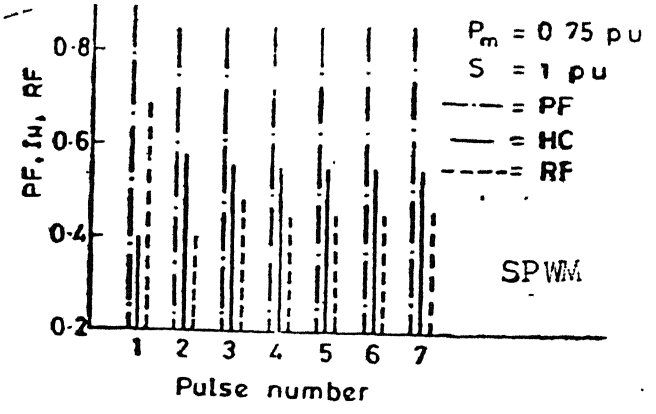


Fig.2.14 Effect of pulse number on power factor, harmonic content and ripple factor

The number of pulses chosen per half cycle have the following influence on the performance characteristics in both the schemes :

(i) Fig. 2.10 shows that the lower order harmonics reduce to a very small values as the pulse number increases. However, after certain number of pulses there will be no appreciable reduction in the lower order harmonic.

(ii) It is evident from Figs. 2.8 - 2.14 that the pulse number beyond three (in the present case) does not offer any additional improvement in the different performance characteristics. On the contrary the higher pulse number will reduce the system efficiency and the control range due to increased switching losses and, finite delay time between two successive commutations respectively.

2.4 CONCLUSIONS

2.4.1 Converter with Constant Load Current

From the above discussion the following important conclusions can be drawn.

1. Among single stage control schemes, scheme 5 the symmetrical single pulse modulation, offers the highest power factor, with reasonably high distortion factor and low lower order harmonics, zero reactive power and unity fundamental p.f. However, voltage ripple factor and second harmonic in output

voltage are only next to fully controlled converter (scheme 1), which has the highest values. Thus while scheme 5 gives the best performance from source consideration, it is the worst from load consideration among all the single stage p.f. control schemes.

2. Among all the single stage control schemes, scheme 4, the two pulse modulation with one forced commutation per half cycle, has the least distortion factor and the p.f. which is only higher than scheme 1. The lower order harmonics in source current are also very high. The load voltage ripple factor is favourable being only a little higher than scheme 7, which has the lowest values. Thus while this scheme offers good performance on load side, the performance on source side is not satisfactory.

3. Among single stage control schemes employing forced commutation, schemes 6,7 and 8 provide a performance which is reasonably good, both on source and load sides. Among these three, scheme 7 has the lowest voltage ripple factor and p.f. which is higher than schemes 1-4. However, the distortion factor is quite low and third harmonic component is only next to scheme 4 (which is highest). Scheme 6 has higher p.f., higher distortion factor, lower third and seventh harmonics and higher voltage ripple factor than scheme 6. Thus as compared to scheme 7, scheme 6 offers slight improvement in performance on source side and slight deterioration performance on load side. As compared to

schemes 6 and 7, scheme 8 has higher PF and distortion factor, higher load voltage ripple factor and zero third harmonic. Thus scheme 8 has better performance at source and inferior performance at load terminals as compared to schemes 6 and 7.

4. Among single stage control schemes employing natural commutation, scheme 2 offers :

(a) power factor which is comparable to scheme 7 but significantly less than that of schemes 6 and 8,

(b) distortion factor which is higher than schemes 6,7 and 8, indicating lower total harmonic context in source current,

(c) third harmonic current is fairly high compared to schemes 6 and 8, however fifth and seventh harmonics are less compared to schemes 6,7 and 8,

(d) voltage ripple factor which is much larger compared to schemes 6 and 7 but quite comparable to scheme 8.

Thus, on the whole scheme 2 offers performance which is inferior compared to schemes 6,7 and 8 but far superior compared to scheme 1. Considering that scheme 2 uses natural commutation, which is reliable, it is fairly competitive compared to schemes 6,7 and 8, and therefore, expected to find wide application.

5. Two stage control in general permits further increase in PF and reduction in lower order harmonics and voltage ripple factor. Scheme 2 with two stage control when compared with schemes 6, 7 and 8, the following points are noted: power factor is higher

distortion factor is much higher and voltage ripple factor is less than in schemes 6 and 8. Thus two stage control of scheme 2 gives a performance which is superior than that of schemes 6,7 and 8.

2.4.2 SPWM and APWM Control of dc Motor

(i) For single pulse/half cycle the asymmetrical PWM scheme has the third harmonic line current and the load current ripple lower than the SPWM scheme. Though the fundamental p.f. is lower, the leading p.f. characteristic of APWM can be usefully employed for partial compensation of lagging loads operating in conjuction with the converter.

(ii) For higher number of pulses there is no difference in performance between the two schemes.

(iii) For pulses more than some number (in the present case 3 pulses) there is no further improvement in the converter performance except shift of harmonic spectrum to higher order. However, the higher number of pulses increase the switching losses.

CHAPTER 3

MODIFIED SEQUENCE CONTROL FOR REGENERATIVE BRIDGE CONVERTERS

.1 INTRODUCTION

As seen in Chapter 2, the fully controlled thyristor onverters which are capable of regeneration, when operated vith the conventional phase-control technique, have three listinct disadvantages, namely, high reactive power consumption (particularly at lower output voltage), generation of relatively large value of lower order line current harmonics, and high ripple in the output voltage. Until now many methods have been reported for improving the performance of regenerative converters. However, sequence control of more than one converter in series appears to be the most promising method (especially for single-phase converters) for improving the performance of converters and therefore widely used in main line traction. In the conventional sequence control [6], the input voltages to the individual bridge converters are equal, reduction in the reactive power is affected by operating the converters in sequence such that, over the range of output, one converter is phase controlled while others are maintained either at full advance (rectification) or full retard (inversion). In [8] an improved sequence control scheme has been

presented, where, unlike in [6], the converter inputs and their sequence of operation are based on the criterion of minimum reactive power over the range of output voltage.

The sequence controls described in [6] and [8] are based on the conventional phase control technique. In this chapter a modified sequence control scheme for single-phase regenerative converters is presented. Using the recently developed control flywheeling technique [11], the fully-controlled converters are operated in the half-controlled mode. The controlled flywheeling retains the regeneration characteristic of the fully-controlled converters and enables the converter to operate with the characteristics of half-controlled converter. In this method, unlike the conventional one, the series connected bridges have unequal ratings (inputs). The control strategy and the converter ratings are such that the maximum reactive power at any output voltage does not exceed the maximum reactive power due to the least rated converter. Two control strategies and a generalised approach of grading the converter input voltages are described.

A comparative evaluation of the proposed method with the following methods is carried out, wherein the conventional phase-control is termed as normal control :

a. Normal Control

1. Single-bridge converter

2. Sequence control of equal rated two bridge converters

3. Sequence control of unequal rated two-bridge converters

b. Controlled Flywheeling

4. Single-bridge converter

5. Sequence control of equal rated two-bridge converters

Comparative evaluation is based on the performance characteristics such as total power factor, dominant line current harmonics, fundamental input current, and voltage ripple in the output voltage. For simplicity, an ideal source and a constant load current are assumed.

3.2 MODIFIED SEQUENCE CONTROL

3.2.1 Reactive Power Consumption in Series-Connected Bridge Converters

Fig. 3.1 shows a single-phase ac-dc converter scheme employing n number of series connected regenerative bridge converters. The secondary-to-primary turns ratios $a_1, a_2, \ldots, a_n$ of n number of secondary windings are such that

$$\sum_{i=1,n} a_i = 1 \qquad (3.1)$$

and $a_1 < a_2 < \ldots < a_n$.

Ratios a_1 to a_n correspond to the normalised voltage or power ratings of the converters.

All the n bridges are operated with the half-controlled characteristic. The average output voltage of the ith bridge, operating at firing angle α_i, is given by

$$V_{di} = \frac{a_i E_m}{\pi} [\pm 1 + \cos\alpha_i] \qquad 0 \leq \alpha_i \leq \pi$$

where positive sign applies to the rectifying mode.
Expressing in per unit, the output voltage

$$r_i = \frac{a_i}{2} (\pm 1 + \cos\alpha_i) \tag{3.2}$$

where $r_i = V_{di}/V_{do}$

$V_{do} = 2E_m/\pi$ (base voltage)

The peak fundamental reactive component of the line current i_{si} (Fig. 3.2) and the fundamental reactive power due to ith bridge are given by

$$I_{qi} = \frac{2a_i I_d}{\pi} \sin\alpha_i$$

and $Q_i = E_m I_{qi}$

Expressing in per unit, the reactive power

$$q_i = \frac{a_i}{2} \sin\alpha_i \tag{3.3}$$

where $q_i = Q_i/Q_{max}$

Q_{max} = maximum reactive power in a single-bridge converter operated with normal control

$= 4I_dE_m/\pi$ (base value)

From eqns. (3.2) and (3.3), the output voltage and reactive power for the ith bridge are related as

$$q_i = [r_i(a_i - r_i)]^{1/2} \tag{3.4}$$

Eqn. (3.4) shows that output voltage and the fundamental reactive power of a bridge are related with an equation of a semicircle. From eqns. (3.2) and (3.4), it is evident that the reactive power demand of the bridge converter is zero when it is at full advance ($\alpha_i = 0$) and full retard ($\alpha_i = \pi$). At $\alpha_i = \pi/2$, the reactive power is maximum and equal to $a_i/2$.

Similarly, the output voltage and reactive power for a single-bridge converter operating with normal phase control are given by

$$r_i = a_i \cos\alpha_i$$

and (3.5)

$$q_i = (a_i^2 - r_i^2)^{1/2}$$

From eqns. (3.1) and (3.2), the total output voltage of n number of series-connected bridges is given by

$$r = \frac{1}{2} \left(\pm 1 + \sum_{i=1}^{n} a_i \cos\alpha_i \right) \qquad (3.6)$$

where positive sign applies to rectification operation and negative sign for inversion operation. Since only one bridge is under α control, while others are maintained either at full advance or full retard, the total reactive power is solely governed by the converter under control. Therefore, from eqn. (3.3), the total reactive power with controlled flywheeling operation is given by

$$q = \frac{a_i}{2} \sin\alpha_i \qquad (3.7)$$

From eqn. (3.7), to keep the reactive power in the whole range of output voltage below $a_1/2$, the turns ratios and the control strategy should be such that

$$\frac{a_1}{2} = \frac{a_i}{2} \sin\alpha_i \qquad (3.8)$$

where $i = 1,2, \ldots, n$.

Eqn. (3.8) reveals that, converter 1 (minimum rated) operates over the full range of firing angle, whereas others operate over the restricted range of firing angles. Method of fixing turns ratios and two sequence control techniques described below are based on eqn. (3.8).

3.2.2 Sequence Control Technique 1

a. Two bridge scheme

Fig. 3.3 shows the reactive power diagrams for single-bridge and two-bridge schemes employing half-controlled characteristic. It explains the effect of cascade connections, grading the bridge inputs, and control sequence on the reactive power demand. The explanation of the figure, for the increase in output voltage from zero to one per unit in rectifying mode, is as follows.

Semicircle 1 and 2-2', respectively, show the reactive power demand in single-bridge (i.e., $a_1 = 1$, $a_2 = 0$) and two-bridge (i.e., $a_1 = a_2 = 0.5$) schemes. The maximum reactive power in the first scheme is 0.5 p.u., while in the latter scheme it is 0.25 p.u. For graded inputs, i.e., $a_1 \neq a_2$, two bridges may be controlled in three possible sequences as described below.

Sequence following Semi-circles 3-4' : For output voltage in the range AB, bridges 1 and 2, respectively, are in the half-controlled mode and at full retard, whereas in the range BE they are at full advance and in half-controlled mode, respectively.

Sequence following the Semi-circles 4-3' : In the range, AD, bridges 1 and 2 are at full retard and in the control mode, respectively, whereas in the range DE, bridges 1 and 2 are

in the control mode and at full advance, respectively.

Modified sequence :

By operating the bridges in a sequence so that the reactive power follows the path described by semicircle 3-arcs BC-CD. Semicircle 3', the maximum reactive power demand can be reduced to a value smaller than $a_2/2$ p.u. To increase the voltage from zero to 1 p.u., the sequence controller has to operate the bridges in the following sequence.

When the output voltage is

i) in the range AB, bridge 1 is under control, and bridge 2 is at full retard ;

ii) in the range BC, bridge 1 is at full retard, while bridge 2 is under control;

iii) at point C', bridges 1 and 2 which were, respectively, at full advance and at firing angle θ_1 are now brought to full retard and firing angle θ_2, respectively, without altering the output voltage, where

$$\theta_1 = \pi - \theta_2 \qquad (3.9)$$

iv) in the range CD, bridge 1 is at full retard, and bridge 2 is under control;

v) in the range DE, bridge 1 is under control, and bridge 2 is at full advance.

When the converters are operated in the manner shown, the reactive power demand has three peaks over the range of output, two of magnitudes $a_1/2$ and one of magnitude CC'. The maximum reactive power can be minimized to $a_1/2$ (reactive power of the lowest rated bridge) by equating the peaks as

$$\frac{a_1}{2} = \frac{a_2}{2} \sin\theta_2 \tag{3.10}$$

At point C', the voltage before and after the changeover are equal. Therefore,

$$a_1 + \frac{a_2}{2}(1+\cos\theta_1) = \frac{a_2}{2}(1+\cos\theta_2) \tag{3.11}$$

From the solution of eqns. (3.1), and (3.9) to (3.11)

$$a_1 = 0.415, \quad a_2 = 0.585, \quad \theta_1 = 135^\circ, \quad \text{and} \quad \theta_2 = 45^\circ .$$

From the reactive power diagram, one may note that the reactive power is zero at four points (A,B,C, and E) in the modified control scheme, whereas it is zero at two and three points in single-bridge and sequence-control ($a_1 = a_2$) scheme, respectively.

The operation of the bridges in the inverter operation can similarly be explained. The control strategy for technique 1 for rectifier operation is given in Fig. 3.4(a).

b. Three bridge scheme

Fig. 3.5 shows the reactive power consumption in a three-bridge scheme for rectifier operation when the output voltage is varied from zero to full value. Semicircle 1 shows reactive power variation for single bridge ($a_1 = 1$). Semicircles 2-2'-2" show the control sequence for $a_1 = a_2 = a_2 = \frac{1}{3}$. The maximum reactive power demand in this case is $a_1/2$. In the case of graded inputs, the three bridges can be operated in five possible sequences. In the first four sequences followed by semicircles 3-4'-5' ; 4-3'-5' ; 5-4"-3"', and 5-3'-4"', the maximum reactive power demand is $a_3/2$.

Modified Sequence :

The maximum reactive power can be kept below $a_3/2$ by confining the reactive power to vary on the trace shown by semicircle 3 - arcs BC-CD-semicircle 3'-arcs EF-FG-semicircle 3" -arc HI-IJ - semicircle 3"'. In the process of controlling the output voltage, the different bridges are to be operated in the sequence given in Table 3.1.

At the points C and F, where the sequence of operations are reversed, the following equations may be written. For output voltage to be the same before and after the reversal, the constraints on the firing angles are

$$\theta_1 = \pi - \theta_2 \qquad (3.12)$$

and

$$\theta_3 = \pi - \theta_4 \qquad (3.13)$$

Table 3.1

Conduction pattern of the bridge converters in a three-bridge scheme

Bridge number and turn ratio of associated winding		Output voltage in the range/at a point							
		AB (GH)	BC (HI)	C (I)	CD (IJ)	DE (JK)	EF	F	FG
1	a_1	CS (CS)	FA (FA)	Change over from FA to FR	FR (FR)	CS (CS)	FA	Change over from FA to FR	FR
2	a_2	FR (FR)	CS (CS)	Change over from θ_1 to θ_2	CS (CS)	FA (FA)	FA		FR
3	a_3	FR (FA)	FR (FA)		FR (FA)	FR (FA)	CS	Change over from θ_3 to θ_4	CS

CS - Control state FR - Fully retarded FA - Fully advanced

Over the output range, the reactive power has seven peaks : four of magnitude $a_1/2$, two of magnitude CC', and one of magnitude FF'. Reactive power can be minimized by equating the peaks. Therefore,

$$\frac{a_1}{2} = \frac{a_2}{2} \sin\theta_2 = \frac{a_3}{2} \sin\theta_3 \qquad (3.14)$$

At point C', and similarly at F', voltages before and after the changeover of bridge operations are equal. Therefore, we have

$$a_1 + \frac{a_2}{2} (1+\cos\theta_1) = \frac{a_2}{2} (1+\cos\theta_2) \qquad (3.15)$$

and

$$a_1 + a_2 + \frac{a_3}{2} (1+\cos\theta_3) = \frac{a_3}{2} (1+\cos\theta_4) \qquad (3.16)$$

The solution of eqns. (3.1) and (3.12) to (3.16) gives

$$a_1 = 0.2, \quad a_2 = 0.28, \quad a_3 = 0.52, \quad \theta_1 = 135^\circ,$$

$$\theta_2 = 45^\circ, \quad \theta_3 = 157.5^\circ, \quad \text{and} \quad \theta_4 = 22.5^\circ .$$

Also, we may note that over the full output range eight points occur at which reactive power is zero.

c. <u>n-Bridge Scheme :</u>

From the knowledge of the equations derived for two- and three-bridge schemes, the generalized equations for n-bridge scheme are derived. At the point of change over of bridge operation, let the firing angle of ith bridge be changed from $\theta_{2.i-3}$ to $\theta_{2.i-2}$. Then

$$\theta_{2.i-3} = \pi - \theta_{2.i-2} \qquad (3.17)$$

where i = 2,3, ..., n .

Equating the peaks of the reactive power,

$$\frac{a_1}{2} = \frac{a_i}{2} \sin \theta_{2.i-2} \qquad (3.18)$$

Equating the output voltages before and after the reversal of sequence for the ith converter,

$$\sum_{j=1}^{i-1} a_j + \frac{a_i}{2} (1+\cos\theta_{2.i-3}) = \frac{a_i}{2} (1+\cos\theta_{2.i-2}) \qquad (3.19)$$

Solution of eqns. (3.1), and (3.17) to (3.19) gives the turns ratiosof the secondary windings and the firing angles at which reversal in the sequence of operation should occur. In an n-bridge scheme, over the range of output voltage, there are 2^n points where reactive power is zero.

3.2.3 Sequence Control Technique 2

Techniques 1 and 2 are basically the same, except the sequence in which different converters are operated. In this technique the turns ratios are the same as in technique 1. The control strategies for two- and three-bridge schemes are discussed below.

a. Two-Bridge Scheme :

i) For voltage within AB (Fig. 3.3), bridge 1 is under control, and bridge 2 is at full retard.

ii) At point B, bridge 2 is fully advanced, and bridge 1 is operated as an inverter with half-controlled characteristic. The firing angle of bridge 1 is adjusted such that voltages before and after the change in sequence remain equal. Therefore,

$$a_2 + \frac{a_1}{2} (\cos\alpha_1 - 1) = a_1 \qquad (3.20)$$

This gives $\alpha_1 = 79.5^\circ$.

iii) In the range BD, bridge 2 is at full advance, and voltage control is obtained by controlling the firing angle of bridge 1 in the range $79.5^\circ \geq a_1 \geq 0$.

iv) In the range DE, bridge 2 is at full advance, and bridge 1 is under control as rectifier.

The control strategy for bridges 1 and 2 are shown in Fig. 3.4(b).

b. Three-bridge scheme :

i) For voltage within the range AD (Fig. 3.5), the control procedure is given by (i) - (iv) in the two-bridge scheme.

ii) At point E, bridges 2 and 3 are brought to full retard and full advance, respectively, and bridge 1 is operated as an inverter with its firing angle adjusted such that

$$a_3 + \frac{a_1}{2} (\cos\alpha_1 - 1) = a_1 + a_2 \qquad (3.21)$$

From eqn. (3.21), $\alpha_1 = 53.1^\circ$.

iii) In EG, bridges 2 and 3 are at full retard and full advance, respectively, and bridge 1 is under control in the inverter mode.

iv) In GH, bridges 2 and 3 are at full retard and full advance, respectively, whereas bridge 1 is under control in the rectifier mode.

v) At point H, bridge 2 and 3 are at full advance, whereas bridge 1, which was at full advance in the rectifier mode, is brought to the inverter mode with its firing angle adjusted such that

$$a_2 + a_3 + \frac{a_1}{2} (\cos\alpha_1 - 1) = a_1 + a_3 \qquad (3.22)$$

From eqn. (3.22), $\alpha_1 = 78.4^{\circ}$.

vi) In HJ and JK intervals, bridges 2 and 3 are at full advance, whereas bridge 1 is controlled as inverter and rectifier, respectively.

3.2.4 Cyclic Firing of the Thyristor Bridge

When the bridge converter, which is operated with the half-controlled characteristic, is in full retard, the load current I_d freewheels through the thyristors connected to the same input terminal, e.g., either pair (S_1, S_4) or (S_2, S_3). Thus the conducting thyristors of the full retarded bridge have to carry I_d continuously, and therefore they need to be rated for current I_d. However, their rating can be reduced to average

current $I_d/2$ by following the cyclic firing of thyristor pairs [22]. To achieve the cyclic firing in bridge 1, the trigger pulses to the thyristors are applied in a manner shown in Fig. 3.6(a). In this, the thyristor pair (S_1,S_4) is fired simultaneously, and 180° later the pair (S_2,S_4) receives the pulses simultaneously. The commutation process is described in Fig. 3.6(b) neglecting the commutation overlap. During a small interval u, the load current flows through the transformer and results in an output voltage v_{d1} which would be negligibly small.

3.3 PERFORMANCE ANALYSIS

In the modified scheme, the different performance criteria for the two-bridge system are computed as follows.

Supply Current Harmonics :

Let I_{s1} and I_{s2} be the supply currents due to bridges 1 and 2, respectively, and let I_s be the total supply current. Fig. 3.2(b) - (d) show their waveforms. Expressing them in harmonic series,

$$i_{s1} = \sum_n a_{n1} \cos n\omega t + \sum_n b_{n1} \sin n\omega t$$

$$i_{s2} = \sum_n a_{n2} \cos n\omega t + \sum_n b_{n2} \sin n\omega t$$

$$i_s = \sum_n a_n \cos n\omega t + \sum_n b_n \sin n\omega t ,$$

where n = 1,3,5, ... order of harmonics.

The Fourier coefficients in per unit of I_d are given by

$$a_{n1} = -\frac{2a_1}{\pi n}\sin n\alpha_1, \qquad b_{n1} = \frac{2a_1}{\pi n}(1+\cos n\alpha_1) \tag{3.23}$$

$$a_{n2} = -\frac{2a_2}{\pi n}\sin n\alpha_2, \qquad b_{n2} = \frac{2a_2}{\pi n}(1+\cos n\alpha_2)$$

$$a_n = a_{n1} + a_{n2}, \qquad b_n = b_{n1} + b_{n2}$$

The rms value of line current harmonic is given by

$$I_n = \left(\frac{a_n^2 + b_n^2}{2}\right)^{1/2} \tag{3.24}$$

From the supply current waveform (Fig. 3.2(d)), the rms supply current in per unit of I_d is given by

$$I_{rms} = \left[\frac{(\alpha_2-\alpha_1)a_1^2 + \pi-\alpha_2}{\pi}\right]^{1/2}, \qquad \text{for } \alpha_1 > \alpha_2$$

$$= \left[\frac{(\alpha_1-\alpha_2)a_2^2 + \pi-\alpha_1}{\pi}\right]^{1/2}, \qquad \text{for } \alpha_1 < \alpha_2 \tag{3.25}$$

The variations of the fundamental and third harmonic currents in the supply, for different schemes under evaluation, are shown in Fig. 3.7(a), (b).

Total Power Factor :

From eqns. (3.24) - (3.25) for n = 1, the total power factor of the supply current is given by

$$PF = \frac{I_1}{I_{rms}}\cos(\tan^{-1} a_1/b_1) \tag{3.26}$$

Fig. 3.7(c) gives the comparative picture of the power factor variation with the output voltage in the proposed and other schemes.

Voltage Ripple Factor :

Fig. 3.2(a) and (d) show the typical waveforms of the rectified output voltage v_d and the load current i_d. As the output voltage is not smooth, load current i_d will have ac ripple superimposed over the average load current I_d. To study the output performance of the converter a voltage ripple factor, which is a measure of the filter choke in the load circuit to limit the current ripple, has been defined in the previous chapter. On the basis of eqns. (2.15) and (2.17), the voltage ripple factor RF for the present case may be derived from

$$R_f = \frac{1}{2\pi} \int_{\psi_1}^{\psi_2} \left(\frac{v_d}{V_{do}} - r\right) d\omega t, \quad v_d > V_d \qquad (3.27)$$

Fig. 3.7(d) shows the variation of RF for the proposed scheme together with the other schemes. It also indicates the value of smoothing inductance in different schemes for a specified current ripple. From the load consideration, the scheme which has lower RF is considered to be better.

3.4 COMPARATIVE EVALUATION

From the study of the performance characteristics in Fig. 3.7 and the reactive power diagrams, the following observations may be made.

Reactive Power Demand :

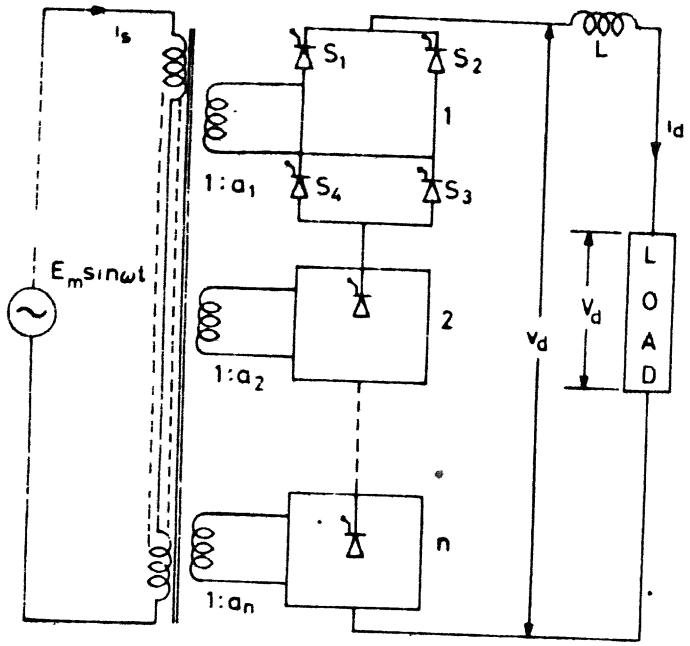
The reactive power is maximum in a single bridge operated with normal control (conventional phase control). Taking this as a base value of 100 percent, the reactive power demands are 50 percent in the conventional sequence control, 41.5 percent in the modified scheme [8], 50 percent in the single bridge with the half-controlled characteristic, 25 percent in a sequence control with half-controlled characteristic, and 20.75 percent in the proposed scheme. Thus, the present scheme will be more effective in reducing the cost of compensators for power factor correction.

Total Power Factor :

A phase-controlled single-bridge has lowest power factor and it declines linearly with output voltage. The modified control scheme offers highest power factor. In the proposed two techniques, technique 2 has better characteristic than 1.

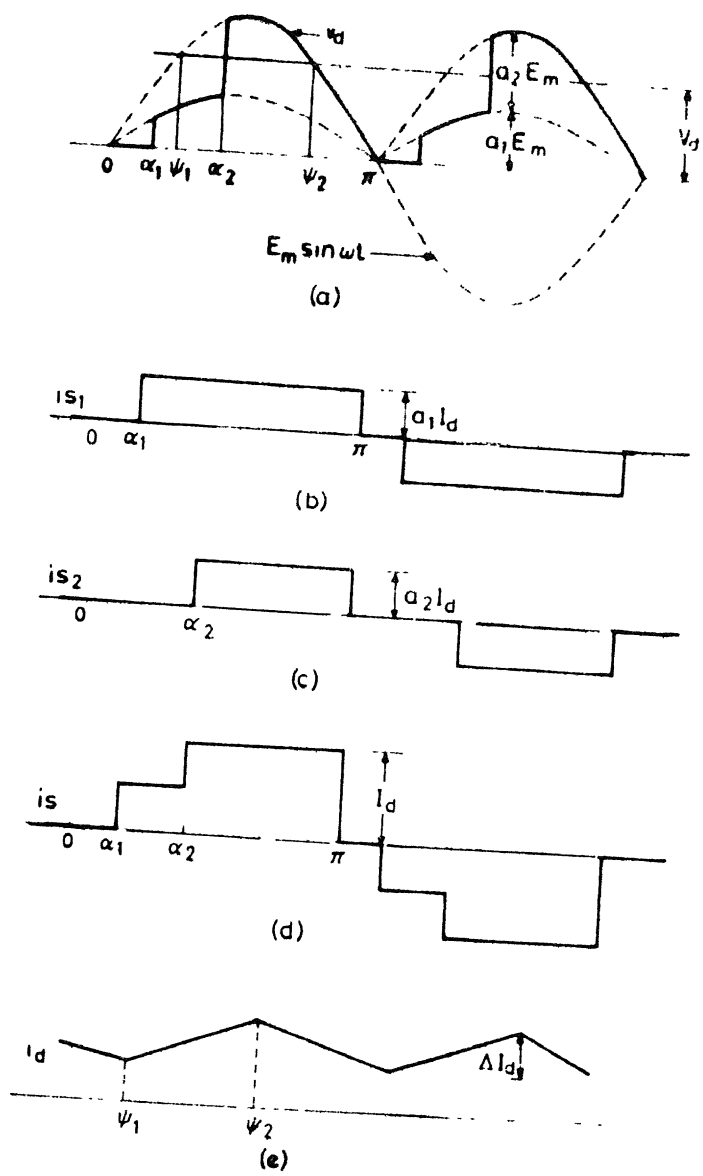
Fundamental Current :

In the case of a phase-controlled single-bridge scheme, the fundamental line current remains constant, whereas in the other schemes it varies with the output voltage. In the proposed techniques it has lower values as compared to other schemes.



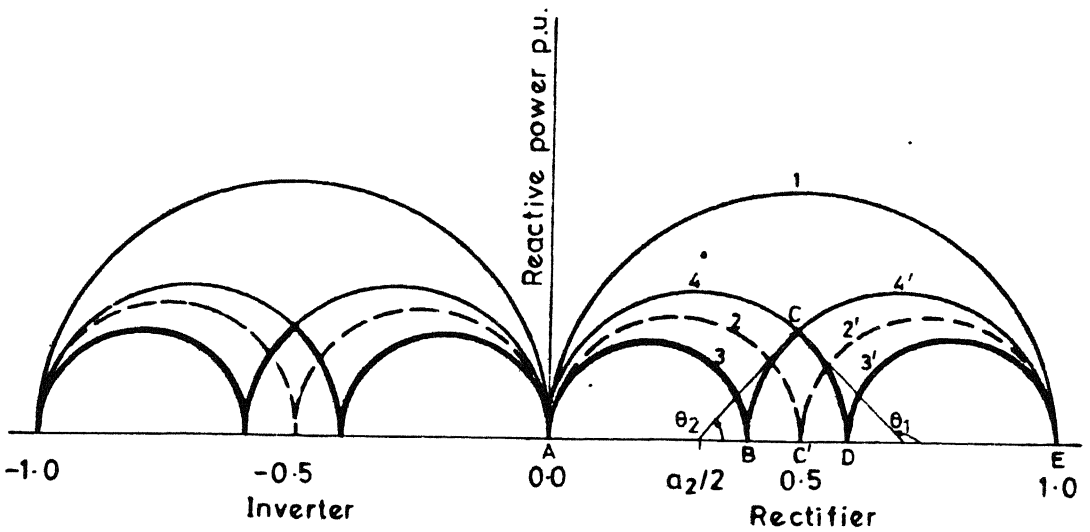
Cascade connection of multi converters

Fig. 3·1



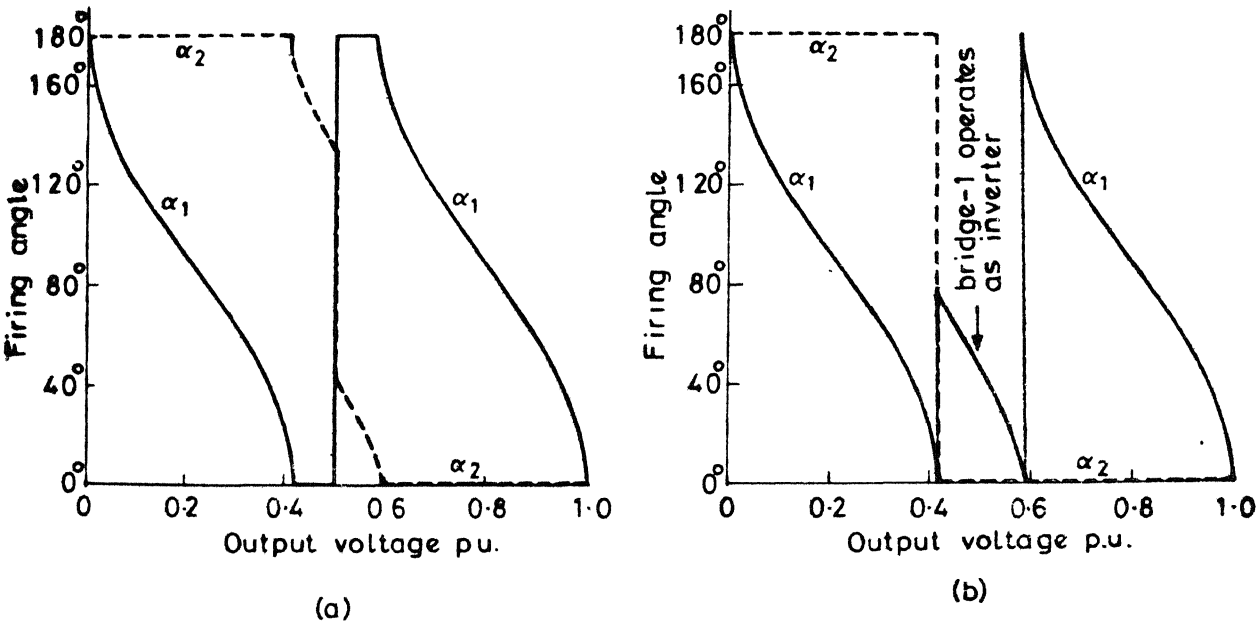
Waveforms (a) output voltage (b) supply current due to converter 1, (c) supply current due to converter 2; (d) total supply current, (e) load current ripple.

Fig. 3-2

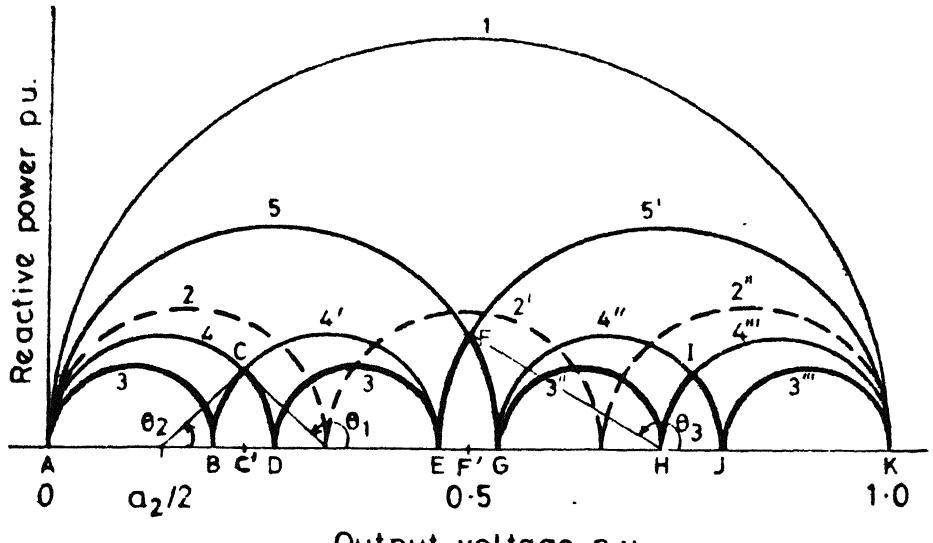


1 Corresponds $a_1 = 1$ 2-2′ Corresponds $a_1 = a_2 = 0.5$
3-3′ Corresponds $a_1 = 0.415$ 4-4′ Corresponds $a_2 = 0.585$

Fig. 3·3 Reactive power consumption in two bridge scheme
Heavy lines show modified control technique I



ig. 3·4 Control strategy: (a) technique 1; (b) technique 2



1 Corresponds $a_1=1$ 2-2'-2'' Corresponds $a_1=a_2=a_3=1/3$
3-3'-3''-3''' Corresponds $a_1=0{\cdot}2$ 4-4'-4''-4''' Corresponds $a_2=0{\cdot}28$
5-5' Corresponds $a_3=0{\cdot}52$

Fig. 3·5 Reactive power consumption in three-bridge scheme Heavy lines show modified control technique I

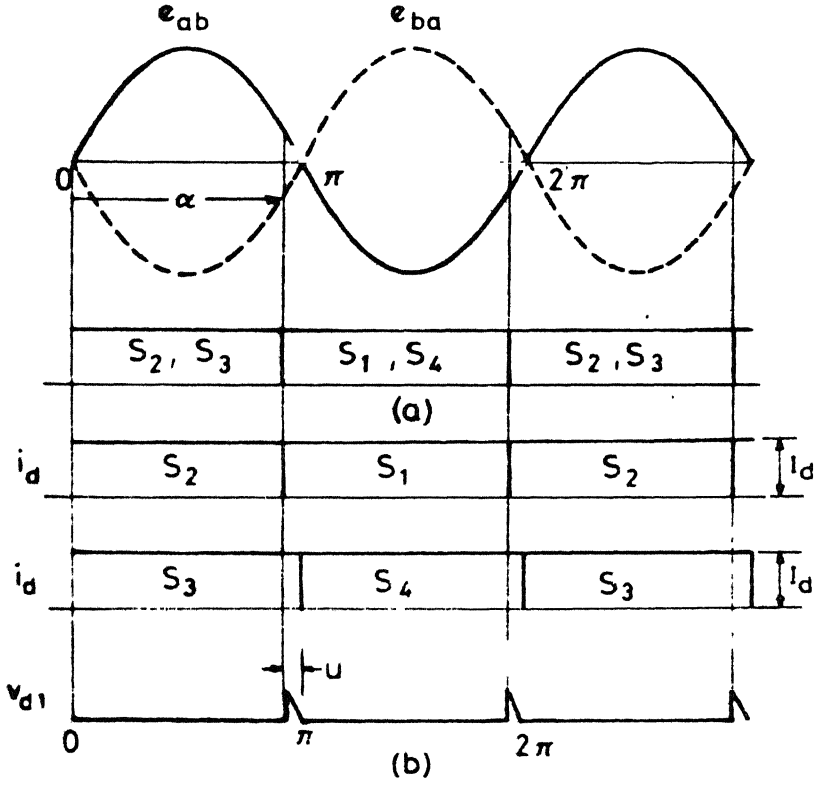


Fig. 3·6 Cyclic firing (a) trigger pulses; (b) current and voltage waveforms in cyclic firing

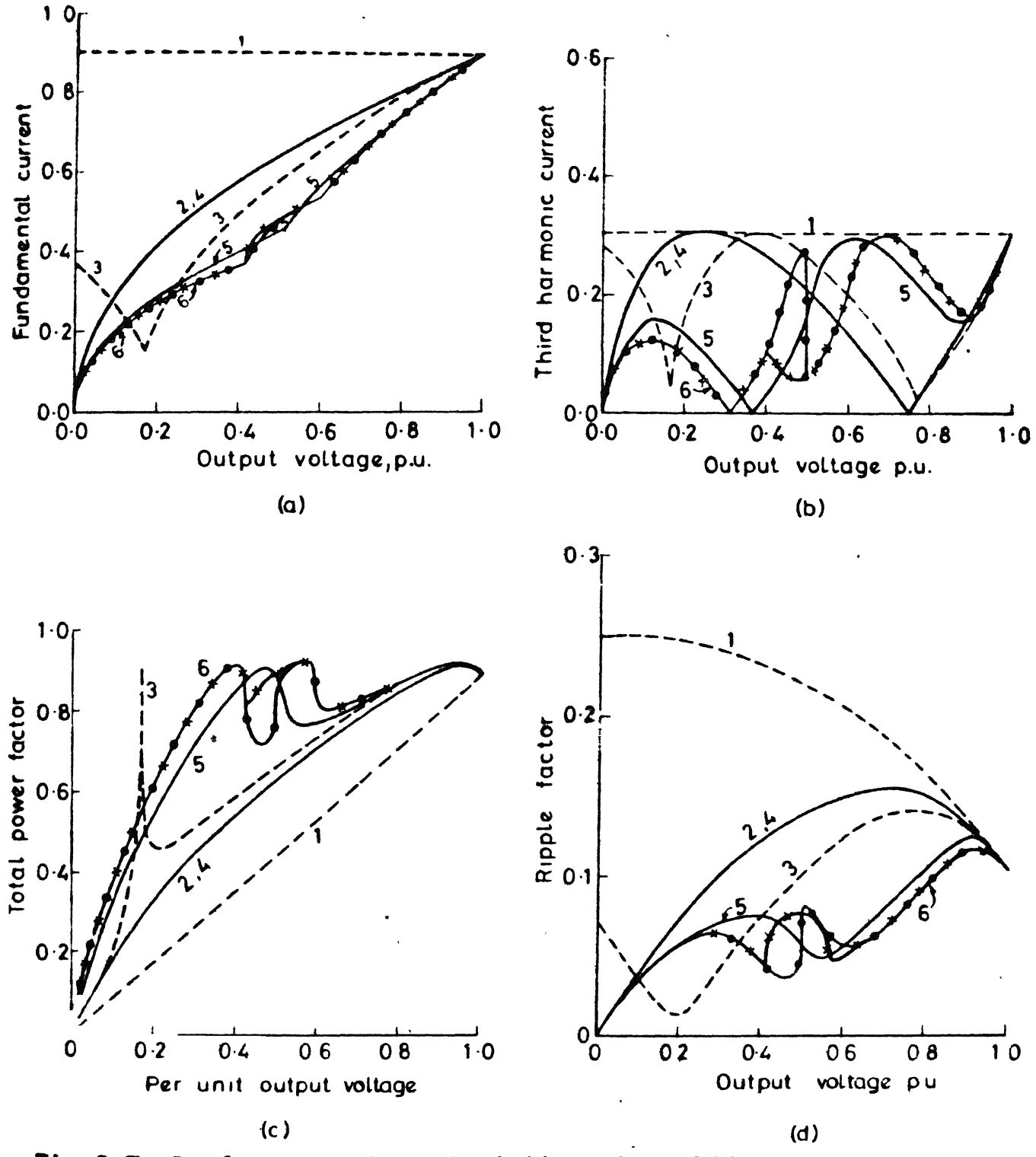


Fig.3.7 Performance characteristics with different control schemes Normal control: 1) single bridge; 2) double bridge; 3) modified scheme (a_1 = 0.415, a_2 = 0.585) [8].Half-controlled characteristic: 4) single bridge; 5) double bridge; 6) proposed techniques (a_1 = 0.415, a_2 = 0.585); -o- is technique 1, -x- is technique 2.

Third Harmonic Current :

In the case of single-bridge with normal control, the harmonic current is of constant amplitude, whereas in other schemes, its magnitudes depends upon the output voltage. In the proposed scheme, the magnitude of the harmonic current, especially in the lower range of the output voltage, is lower compared to other schemes.

Output Voltage Ripple :

Highest voltage ripple is produced in a single bridge converter, operated with normal control. Whereas, in the modified scheme ripple is lowest and has value about 50 percent of the conventional one. This allows a corresponding reduction in the size of the smoothing inductor.

3.5 CONCLUSION

New control strategies have been presented for the sequence control of the series-connected regenerative converters operated with the half-controlled characteristic. A generalised method is given for selecting the turns ratios of the secondary windings of the transformer so that the maximum reactive power can be minimized. The comparative study of different schemes, based on various aspects of the converter performance, shows that the proposed scheme offers better input and output performance, while retaining the regeneration capability. Due to less reactive power consumption and less ripple in the output voltage,

the present scheme may prove to be more economical in reducing the cost of filter inductor and reactive power compensators. This scheme can be advantageously applied to slip-power recovery scheme for slip-ring induction motors, high powered dc drives, and single-phase ac-dc tractions requiring regeneration in the ac lines. However, the present scheme increases the complexity in the control circuit.

CHAPTER 4

SELECTIVE HARMONIC ELIMINATION IN AC-DC CONVERTERS

4.1 INTRODUCTION

By operating the converter at unity displacement factor (fundamental power factor) and minimising the lower order harmonics, the need of external reactive power compensator can be avoided and the cost of the harmonic filters may be minimised. Further, in certain applications like carrier protection in power systems and signalling in electric traction systems it is desirable to suppress those harmonics which are close to signal frequencies. In this context, the forced-commutated converters are better placed over the line-commutated ones as the former ones can be operated at unity displacement factor and the lower order harmonics may be minimised by pulse width control.

In this chapter, a pulse width control scheme for elimination of selective line current harmonics is presented. The proposed method employs suitably placed odd number of pulses per half cycle and the control of the output voltage is affected by varying the pulse widths symmetrically around the pulse positions. The proposed method is compared with the alternative method [31] which employs even number of pulses per half cycle. Control circuit for the implementation of the proposed scheme is presented.

4.2 GENERALISED METHOD FOR ELIMINATION OF M HARMONIC COMPONENTS FROM THE LINE CURRENT

Fig. 4.1 shows the ac-dc converter circuit operating on forced-commutation. The load voltage and line current waveforms are shown in Figs. 4.2. The load current has been assumed to be perfect dc. The operation of the converter is described later. Line current consists of P pulses of equal widths per half cycle. The pulses are located symmetrically around $\pi/2$ axis at the locations $B_1, B_2, \ldots, B_P$, where

$$P = 2M+1 \qquad \text{for P odd} \tag{4.1}$$

$$P = 2M \qquad \text{for P even} \tag{4.2}$$

and M is the number of harmonics to be eliminated. From Fig. 4.2, for the ith pulse,

$$\alpha_i = B_i - d, \qquad i = 1 \text{ to } P \tag{4.3}$$

$$\beta_i = B_i + d$$

and for P odd : $B_{P+1-i} = \pi - B_i, \quad i = 1 \text{ to } M$ (4.4)

$$B_{M+1} = \pi/2$$

for P even : $B_{P+1-i} = \pi - B_i \quad i = 1 \text{ to } M$ (4.5)

From the harmonic analysis of the line current

$$a_n = 0$$

and $$b_n = \frac{8}{n\pi} \sin nd \left(\sum_{i=1}^{M} \sin nB_i + \frac{K}{2} \sin \frac{n\pi}{2} \right) \tag{4.6}$$

where $n = 1,3,5, \ldots$

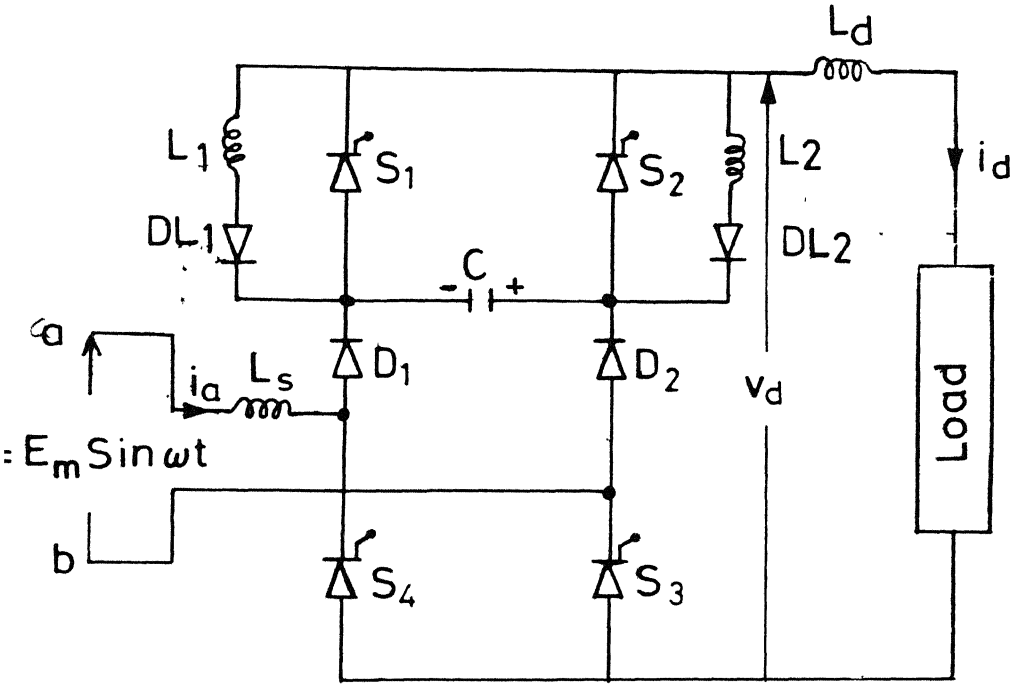


Fig.4·1 Force commutated ac-dc converter

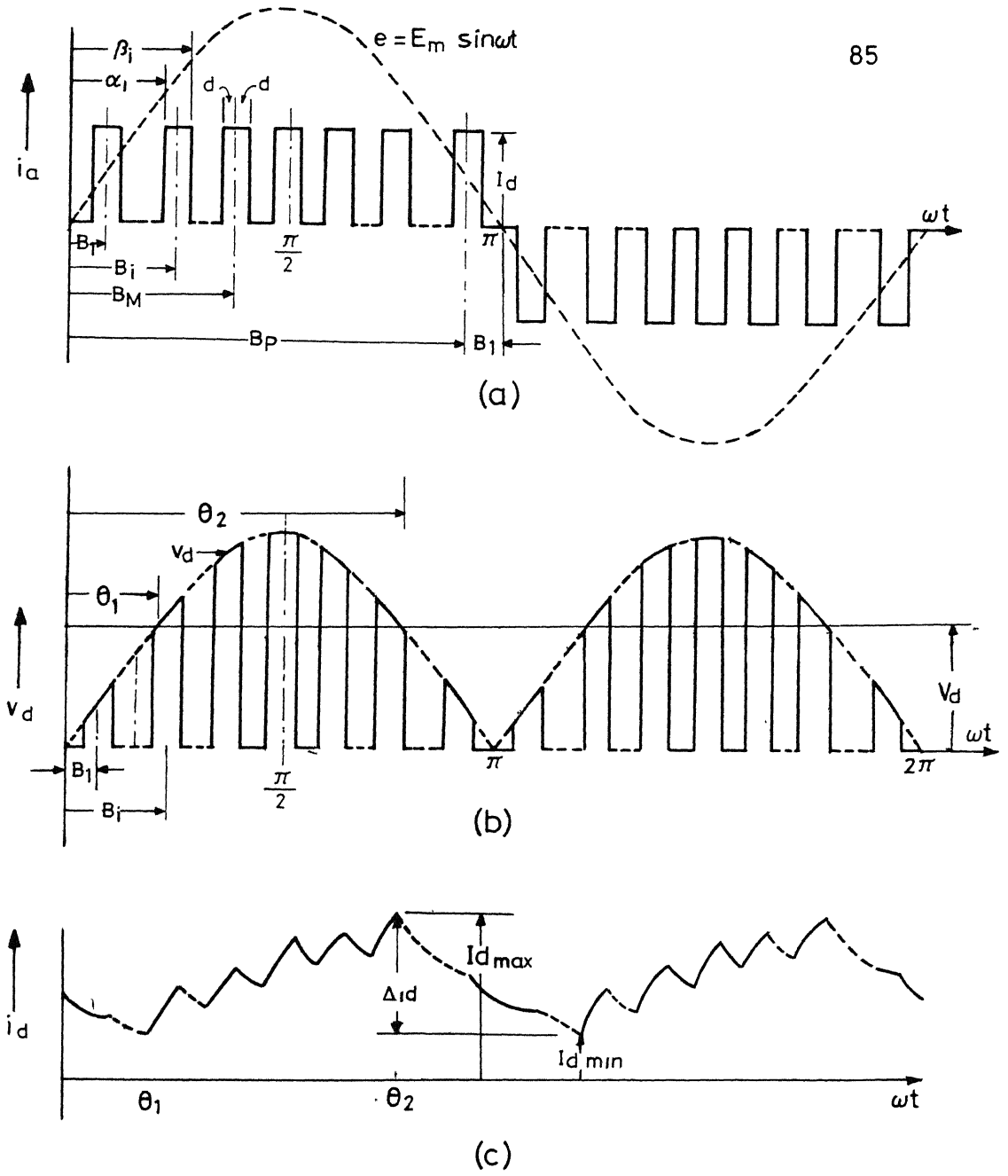


Fig.4·2(a) Ideal line current waveform
(b) Output voltage waveform
(c) Typical load current waveform

and $K = 1$ for P odd (4.7)

$= 0$ for P even

From eqn. (4.7), the necessary conditions for elimination of M harmonics are given by

$$\sum_{i=1}^{M} \sin n B_i + \frac{K}{2} \sin \frac{n\pi}{2} = 0 \qquad (4.8)$$

with the constraints

$$B_1 < B_2 < \ldots < B_M < \pi/2$$

where $n = n_1, n_2, \ldots, n_M$, i.e., the order of the harmonics to be eliminated.

Eqn. (4.8) may be solved numerically for $B_1, B_2, \ldots, B_M$.

4.2.1 Examples of Harmonic Elimination

Let 3rd and 5th harmonics are to be eliminated using odd number of pulses/half cycle. Here, $K = 1$, $M = 2$, $n_1 = 3$ and $n_2 = 5$. From eqn. (4.8)

$$\sin 3B_1 + \sin 3B_2 - 0.5 = 0 \qquad (4.9)$$

$$\sin 5B_1 + \sin 5B_2 + 0.5 = 0 \qquad (4.10)$$

with the constraints

$$B_1 < B_2 < \pi/2$$

Solving eqns. (4.9) and (4.10) by Newton-Raphson numerical method we get

$$B_1 = 37.95^\circ \quad \text{and} \quad B_2 = 68.13^\circ$$

Similarly, for elimination of 3rd harmonic only

$$B_1 = 50^\circ$$

and for 3rd, 5th and 7th harmonics elimination

$$B_1 = 31.65^\circ, \quad B_2 = 57.48^\circ \quad \text{and} \quad B_3 = 72.96^\circ .$$

4.3 PERFORMANCE MEASURES

From Fig. 4.2(b) the average output V_d is given by

$$V_d = \frac{V_{do}}{2} \sum_{i=1}^{P} (\cos\alpha_i - \cos\beta_i)$$

$$= V_{do} \text{ sinnd } (2 \sum_{i=1}^{M} \sin B_i + K) \qquad (4.11)$$

The voltage ratio r is defined as

$$r = V_d/V_{do}$$

$$= \text{sinnd } (2 \sum_{i=1}^{M} \text{sinn} B_i + K) \qquad (4.12)$$

a. Input performance

From Fig. 4.2(a) the rms value of the line current is given by

$$I_{rms} = (\frac{2dP}{\pi})^{1/2} \qquad (4.13)$$

From eqn. (4.6) the rms values of fundamental and harmonic line currents normalized with respect to I_d are given by

$$I_1 = \frac{8}{\sqrt{2}.\pi} \sin d \left(\sum_{i=1}^{M} \sin B_i + \frac{K}{2} \right) \qquad (4.14)$$

and $$I_n = b_n/\sqrt{2} \qquad (4.15)$$

Line power factor is given as

$$p.f. = I_1/I_{rms} \qquad (4.16)$$

b. Output performance

Because of the finite inductance in the load circuit, the load current will not be a perfect dc, as assumed, but it will have ac ripple superimposed on dc as shown in Fig. 4.2(c). This ripple adversely affects the performance of dc motors. A voltage ripple factor as a measure of converter output performance has been defined in Section 2.1. The maximum and minimum values of R_f may be obtained by integrating eqn. (2.15) over the range θ_1 and θ_2 to determine ripple factor RF as defined in eqn. (2.17), where

$$\theta_1 = \sin^{-1} \frac{2r}{\pi} \quad \text{and} \quad \theta_2 = \pi - \theta_1 \qquad (4.17)$$

4.4 COMPARISON OF HARMONIC ELIMINATION METHODS

Converter performance for two selective harmonic elimination methods, viz., with odd number of pulses (proposed method) and using even number of pulses (alternative method) have been compared for the following cases :

(1) 3rd harmonic elimination

(2) 3rd and 5th harmonics elimination

(3) 3rd,5th and 7th harmonics elimination .

Fig. 4.3 shows the variation of power factor and fundamental current for the above three cases for both the methods. Figs. 4.4(a), (b) and (c) show the harmonic variation for first, second and third case respectively. Fig. 4.5 shows the variation of ripple factor in the above cases.

Table 4.1 presents a detailed comparative picture of both the methods. The following important points can be noted :

(i) As seen in Fig. 4.3, the power factor and the fundamental component of the line current remain the same in both the methods and they are independent of the number of harmonics being eliminated. This indicates that the total harmonic distortion of the line current remains the same in both the methods.

(ii) The magnitudes (from the table) of the low-order dominant harmonics in the proposed method are much lower. This will reduce the size of the filter and thereby the power losses in the filter circuit. Although, the switching losses in the proposed method will be little higher due to an additional pulse, the reduction in the filter losses may result in net reduction in the power losses.

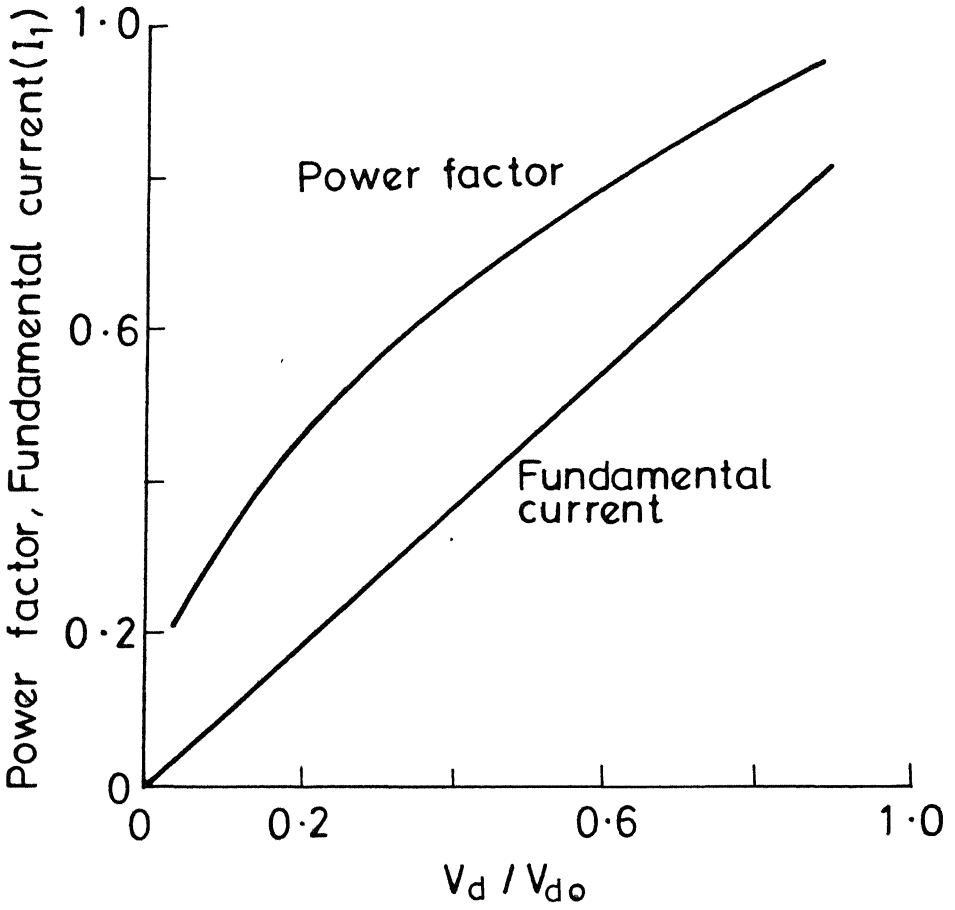


Fig.4·3 Variation of power factor and normalised rms fundamental current for all the three cases in both the methods

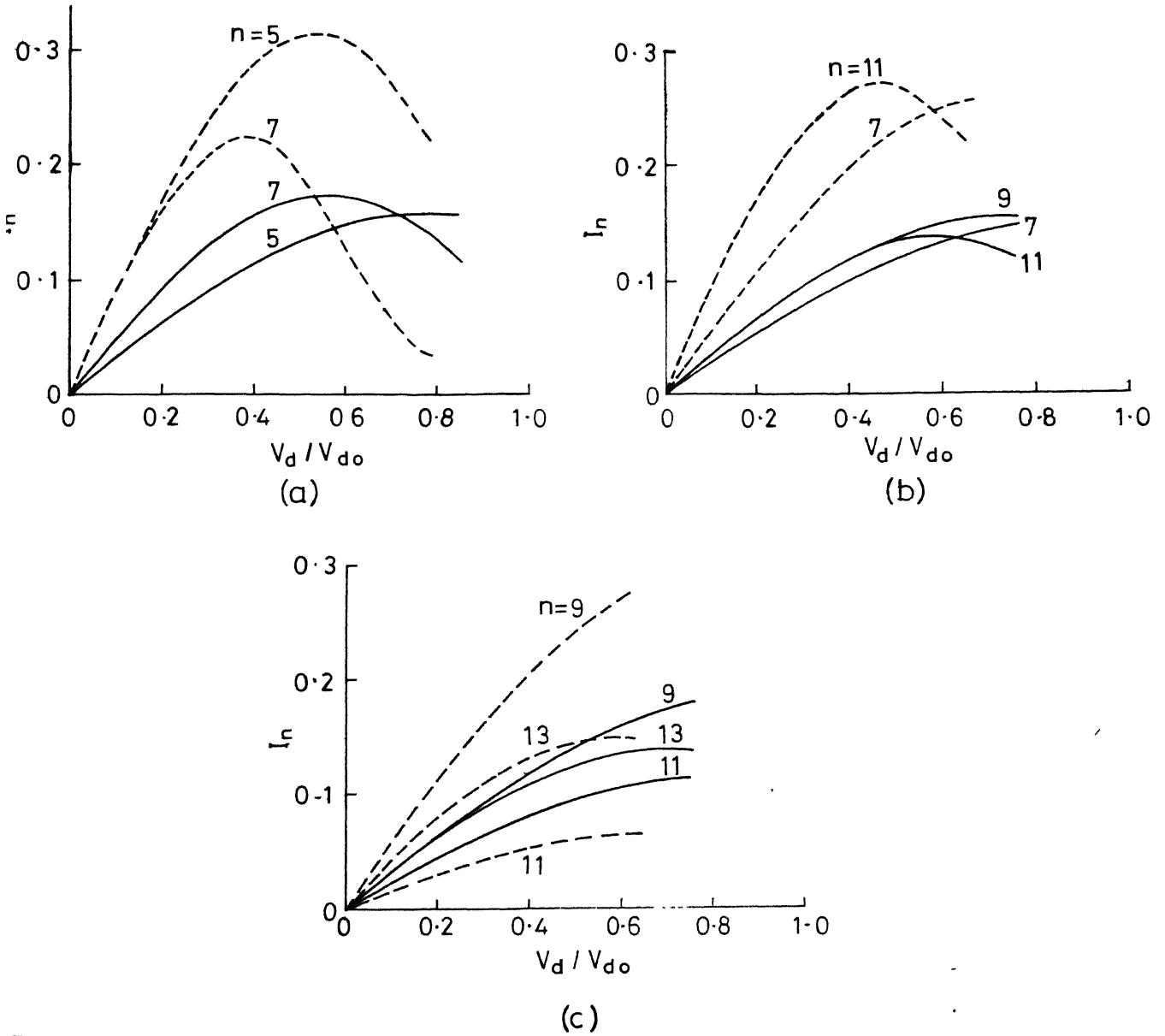


Fig. 4·4 Variation of normalised rms harmonic currents
—— Proposed scheme
---- Alternative Scheme
(a) 3rd harmonic elimination
(b) 3rd and 5th harmonics elimination
(c) 3rd, 5th and 7th harmonics elimination

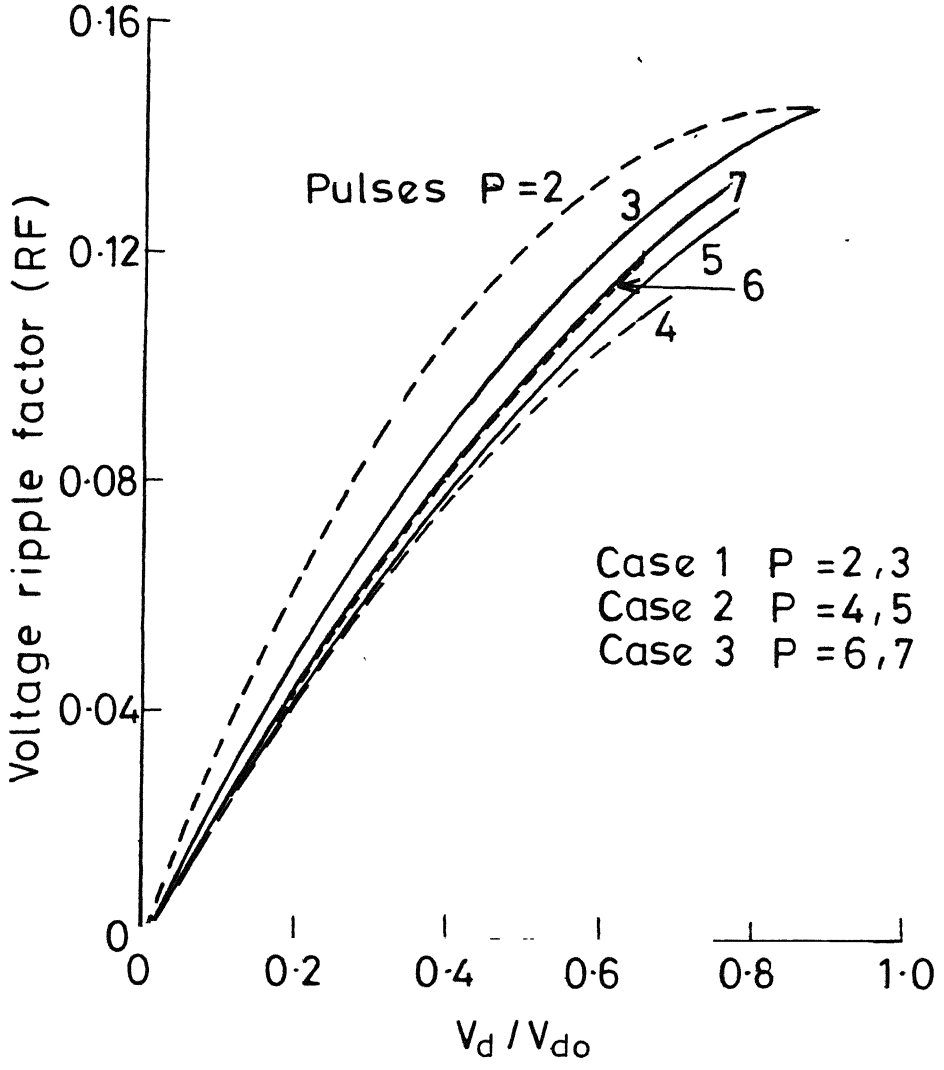


Fig.4·5 Variation of voltage ripple factor

——— Proposed scheme

----- Alternative Scheme

Table 4.1

Line current harmonics in selective harmonic elimination schemes

Order of harmonic	Maximum rms harmonic current as a percentage of load current					
	3rd harmonic elimination		3rd,5th harmonics elimination		3rd,5th and 7th harmonics elimination	
	Proposed method P = 3	Alternative method P = 2	Proposed method P = 5	Alternative method P = 4	Proposed method P = 7	Alternative method P = 6
3	0	0	0	0	0	0
5	15.8	31.2	0	0	0	0
7	17.3	22.2	15	26	0	0
9	30	0	15.5	0	17.6	27.8
11	11	14	13.6	27	11.4	6.5
13	6	11	20.4	14	13.7	15
15	0	0	22	0	15.2	9.5
Maximum output voltage	$.866V_{do}$	$0.866V_{do}$	$.775V_{do}$	$.685V_{do}$	$.76V_{do}$	$.645V_{do}$

(iii) From the table it can be seen that the maximum control range of the output voltage in the case 1 is the same for both the methods, however, for the cases 2 and 3 the proposed method has a higher control range.

(iv) For the case 1, the proposed method has lower voltage ripple factor. However, with the increase in the number of pulses per half cycle, involving elimination of two or more harmonics, ripple factor has nearly the same value.

4.5 AC-DC CONVERTER FOR EXPERIMENTATION

Fig. 4.1 shows the forced-commutated regenerative ac-dc converter circuit [17] for implementing the proposed method. Thyristors S_1-S_4 form a usual bridge circuit. Capacitor C and reactors L_1 and L_2 ($L_1 = L_2$) form a commutation circuit to commutate S_1 and S_2 alternately. Diodes D_1,D_2,D_{L1} and D_{L2} prevent the capacitor from losing the charge. S_1 and S_2 need to be made on and off several times in each half cycle of the line voltage and therefore they must be of inverter grade, whereas S_3 and S_4 are commutated by ac line and therefore they may be of converter grade. Series inductance L_s serves in securing enough commutation voltage across C, especially when the instantaneous line voltage is low. In the positive half-cycle when line 'a' goes positive, the circuit operation in rectifier mode is explained as follows.

Let S_1,D_1 and S_2 are conducting. The load current I_d is assumed to be constant. Let the capacitor be charged with the polarity shown in the figure during the previous commutation.

When S_2 is triggered,S_1 is turned off due to reverse bias provided by the capacitor C. During the commutation interval, C reverses its polarity through the resonant loop C-S_2-L_1-D_1-C and through the load circuit C-S_2-load-S_3-source-C. When the capacitor voltage reaches the line voltage, D_2 comes into conduction and in course of time the load current gets transferred from the source to D_2. Now load current freewheels through S_2,D_2 and S_3.

Similarly, when S_1 is triggered, C, which has reverse polarity, turns off S_2. C reverses its polarity through the resonant circuit constituting L_2 and C and through the load via S_3,D_2 and S_1. D_1 becomes on when the capacitor voltage becomes equal to the source voltage, and D_2 is turned off when the load current rises to I_d.

4.6 CONTROL CIRCUIT FOR THE REALISATION OF FIVE PULSES PER HALF-CYCLE

Fig. 4.6 shows the block schematic of the proposed control circuit. The principle of operation is illustrated in Figs. 4.7(a)-(c).

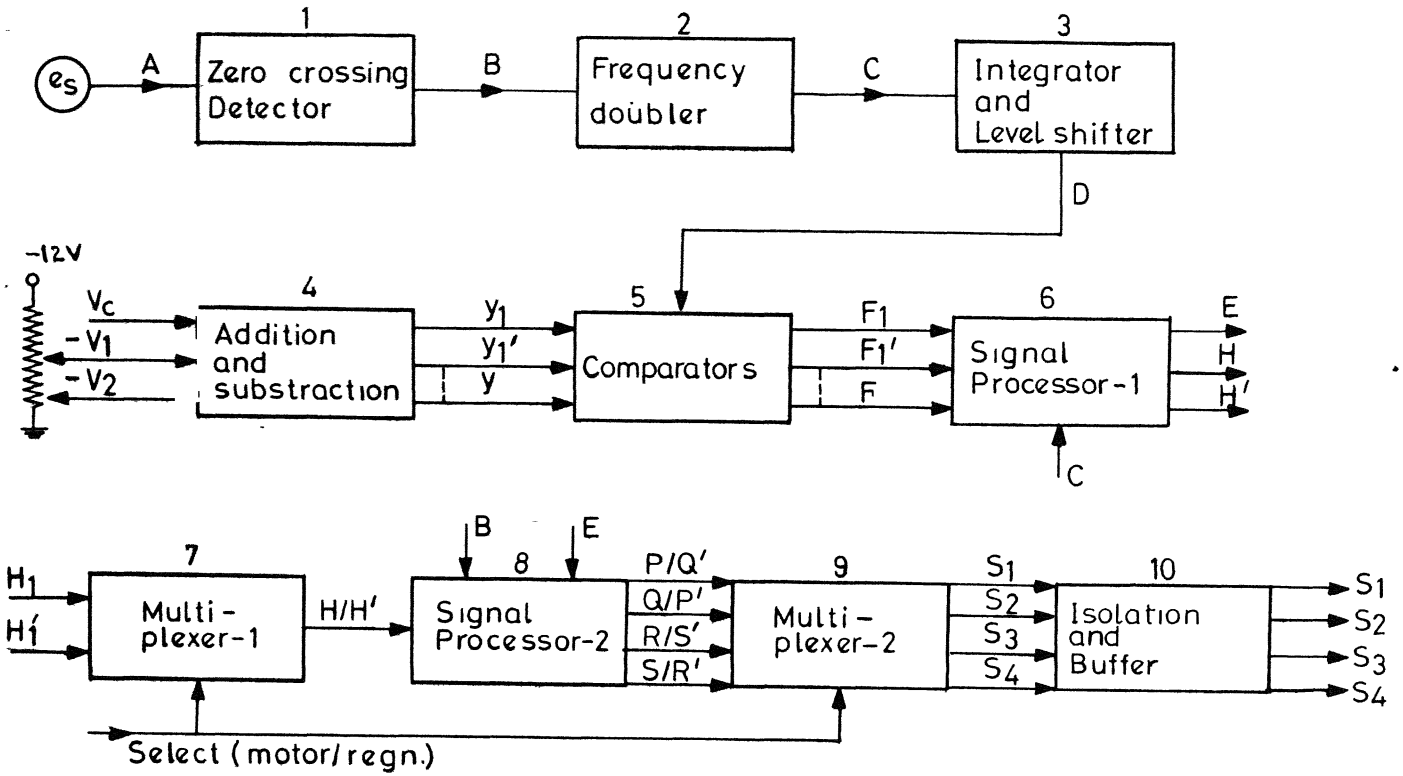
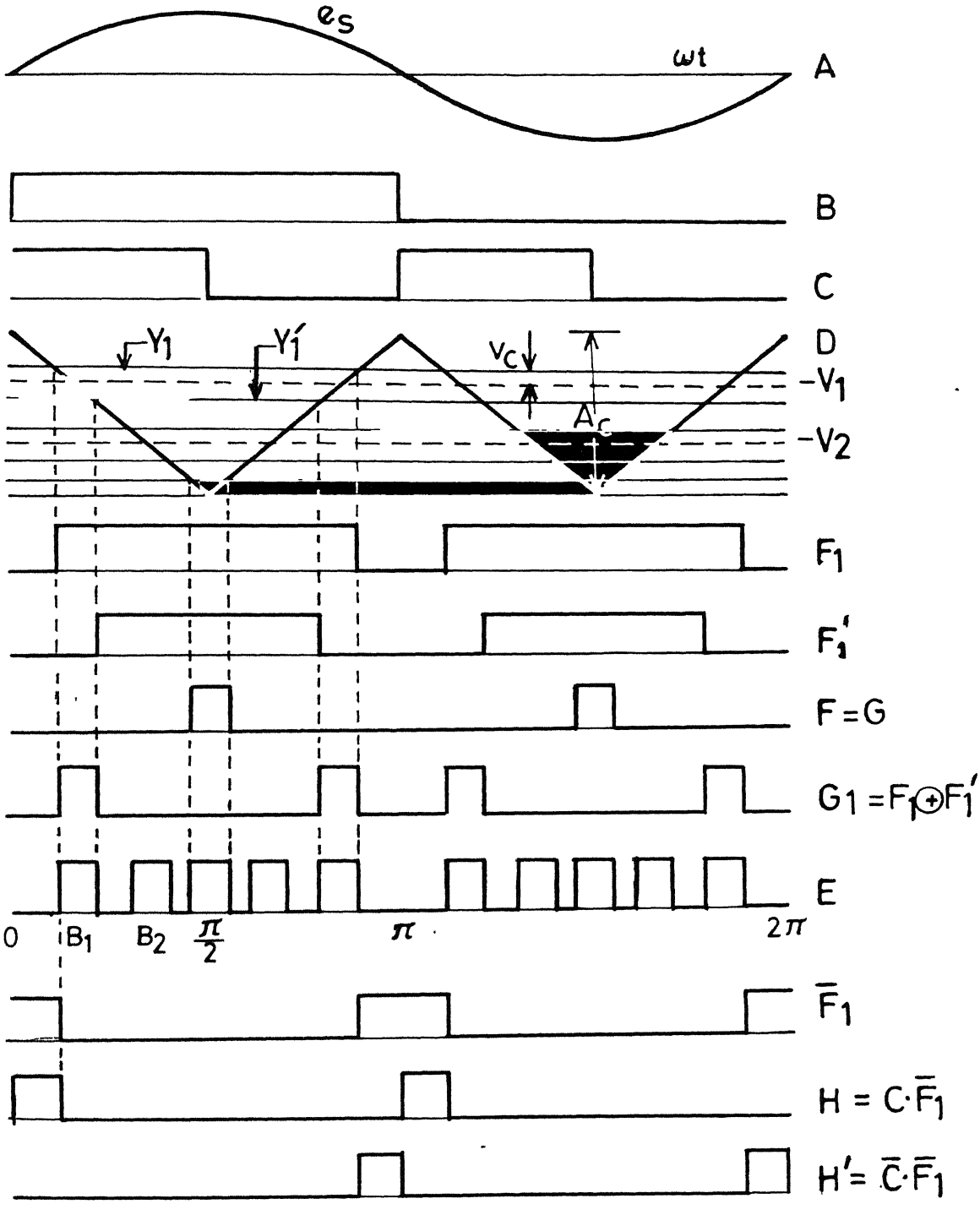


Fig.4·6 Block diagram of the control scheme



g. 4·7(a) Timing diagram of blocks1-6

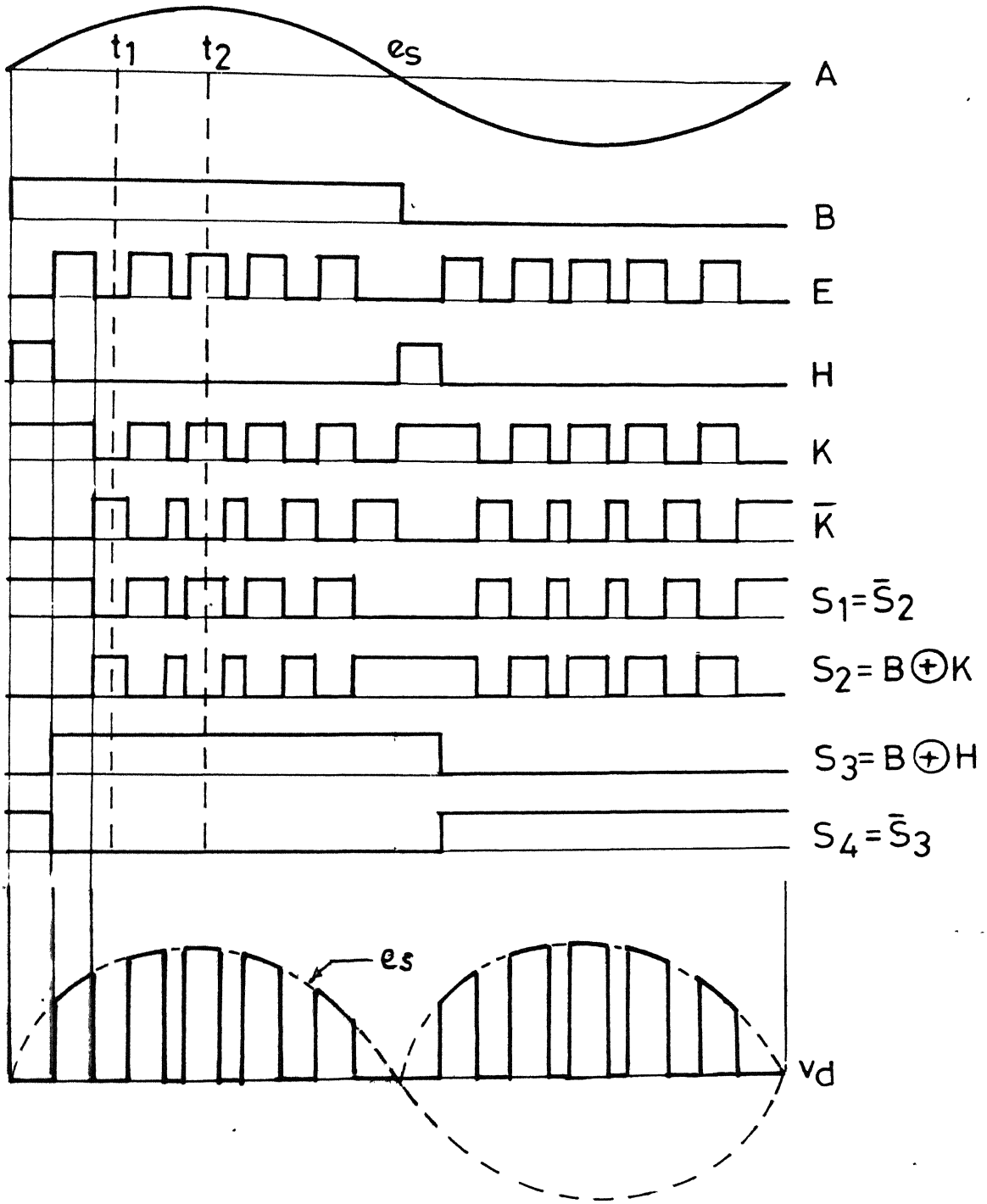


Fig.4·7(b) Timing diagram of blocks7-10 (Rectification)

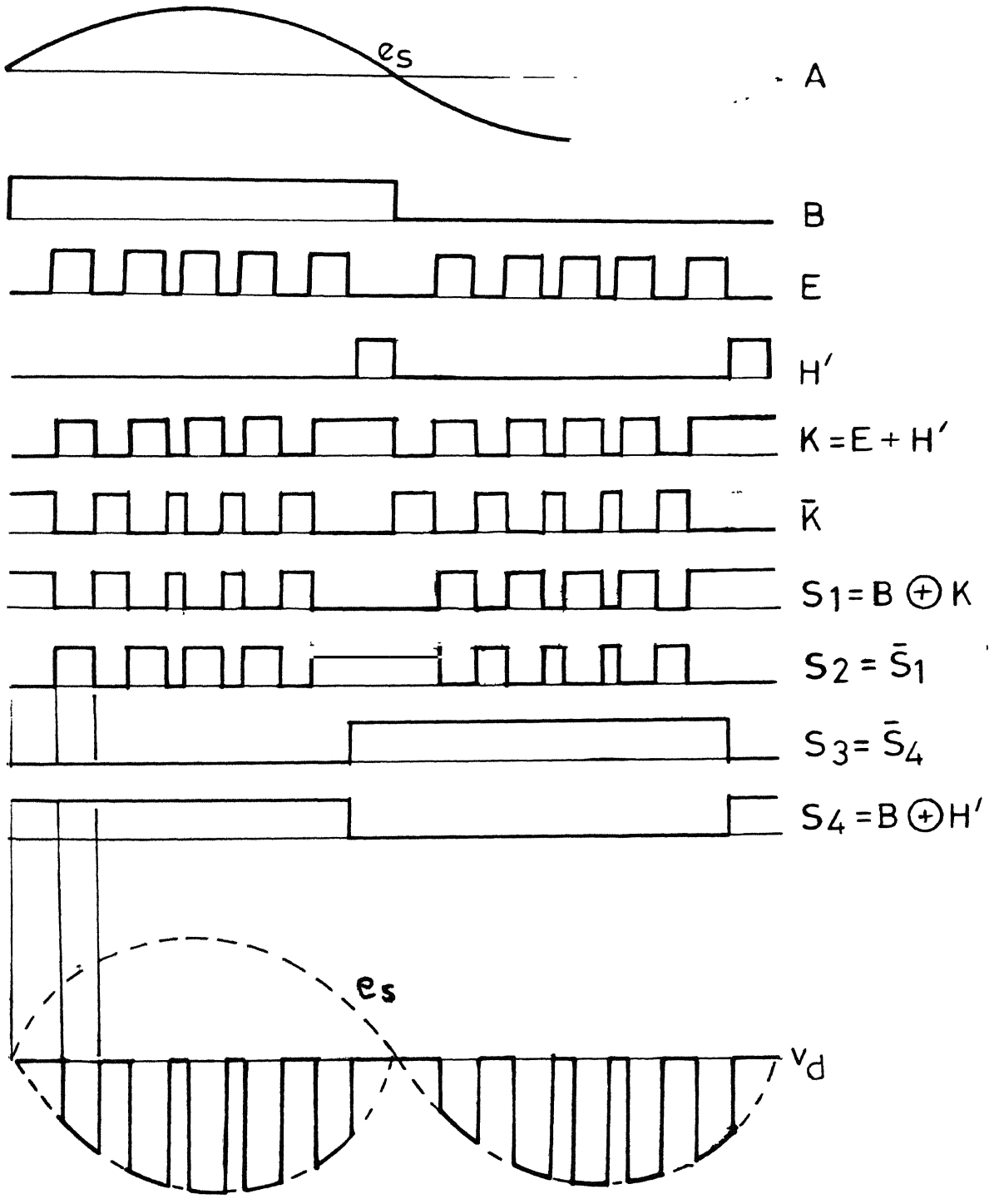


Fig. 4·7(c) Timing diagram of 7 - 10 (Regeneration)

The synchronising voltage A, in phase and proportional to the line voltage, is digitized to a square wave B. The frequency of B is multiplied by two to obtain C which is integrated and then level shifted to generate a triangular wave D of supply frequency and constant amplitude A_c.

For a general case of P pulses per half cycle, the addition and subtraction block comprises P (= 2M+1) amplifiers to deliver the following P outputs :

$$y_i = V_i + v_c \qquad i = 1 \text{ to } M$$

$$y_i' = V_i - v_c$$

and $$y = v_c$$

where the M+1 preset levels $V_1, V_2, \ldots, V_M$ and O, which fix the pulse positions $B_1, B_2, \ldots, B_M$ and $\pi/2$ respectively, are fixed as

$$V_i = \frac{2}{\pi} B_i A_c, \qquad i = 1 \text{ to } M$$

and the control voltage v_c, which varies the pulse widths symmetrically around the pulse positions, is related with the pulse width as

$$v_c/A_c = d/(\pi/2)$$

Voltage levels y, y_1, y_1' etc. are compared with the triangular wave to generate F, F_1, F_1' etc. respectively, which in turn are logically routed to generate E. In the latter part, E is used

to generate the required gate pulses. The pulse width of E corresponds to the interval during which the load remains connected with the input lines and for the rest of the interval load current freewheels.

With proper logics, H and H' are derived from C and F_1. Employing B,E,H and H' the gate pulses are constructed to provide the following features :

(i) Adequacy of rectifying as well as regenerative operation

(ii) Avoidance of retriggering of thyristors during discontinuous load current

(iii) Avoidance of precharging the commutating capacitor at the initial start of the converter.

These features are described below.

a. Rectifying Operation

With 'select' high, converter operates in the rectification mode. Output H of the multiplexer-1 is routed with B and E to deliver P,Q,R and S which appear at the output of the multiplexer-2 as S_1,S_2,S_3 and S_4 respectively, as shown in Fig. 4.7(b). After amplification and isolation through pulse transformers these pulses appear at the respective thyristor gates.

Due to wider gate pulses as shown in the figure, retriggering of the thyristors in the case of discontinuous load

current could be avoided. For example, thyristors S_2 and S_3 when freewheeling the load current, will become off when the load current goes to zero. Next, when S_1 is triggered to power the load, S_4 also needs to be triggered simultaneously if the gate pulses S_4 are of narrow width.

b. Regenerative Operation

In regeneration mode, the 'select' input is at low level. Here, H' is routed with B and E to produce P',Q',R' and S' which in turn appear as S_1,S_2,S_3 and S_4 respectively at the output of multiplexer-2. After amplification and isolation, pulses S_1-S_4 appear at the gates of the thyristors S_1-S_4 respectively (Fig. 4.7(c)).

c. Converter starting without Capacitor Precharging

Assume that the line voltage to the converter is switched on at t = 0 when the line terminal 'a' goes to positive, and at latter time the control circuit is activated in one case at $t = t_1$ and in other case at $t = t_2$ as shown in Fig. 4.7(b). Converter starting for these two different cases is as follows.

Case 1

At $t = t_1$, the gate pulses at thyristors S_2 and S_3 cause capacitor charging through the load via D_1. On occurrence of gate pulse to the thyristor S_1, S_1 turns on and it turns off S_2

by placing the reverse biased capacitor across S_2. Capacitor reverses its polarity and the normal sequence of operations as described earlier will be followed thereafter.

Case 2

At $t = t_2$, due to the presence of gate pulses, S_1 and S_3 become on and they connect the load to the supply. As C remains shorted by conducting thyristors S_1, S_1 cannot be turned off upto $\omega t = \pi$. In the negative half cycle, when the diode D_2 becomes forward biased, load current gets commutated from D_1 to D_2 and the capacitor gets charged with the reverse polarity. This turns off S_1 by placing reverse biased capacitor across S_1, and C reverses its polarity through S_2, L_1 and D_1. Thereafter, the thyristors operate with the normal sequence.

4.6.1 Control Circuit Details

Figs. 4.8(a) and (b) show the detailed circuit diagrams of the control circuit used to realise five pulses/half cycle.

The sinusoidal voltage A is converted into a square wave B using opto-isolator which provides adequate isolation between the power and control circuits. PLL and divide by two counter in the feedback loop multiply the frequency of B by a factor of two. C of twice the supply frequency is integrated by op-amp. The integrated output is level shifted and then amplified using op-amp to generate a triangular wave D of

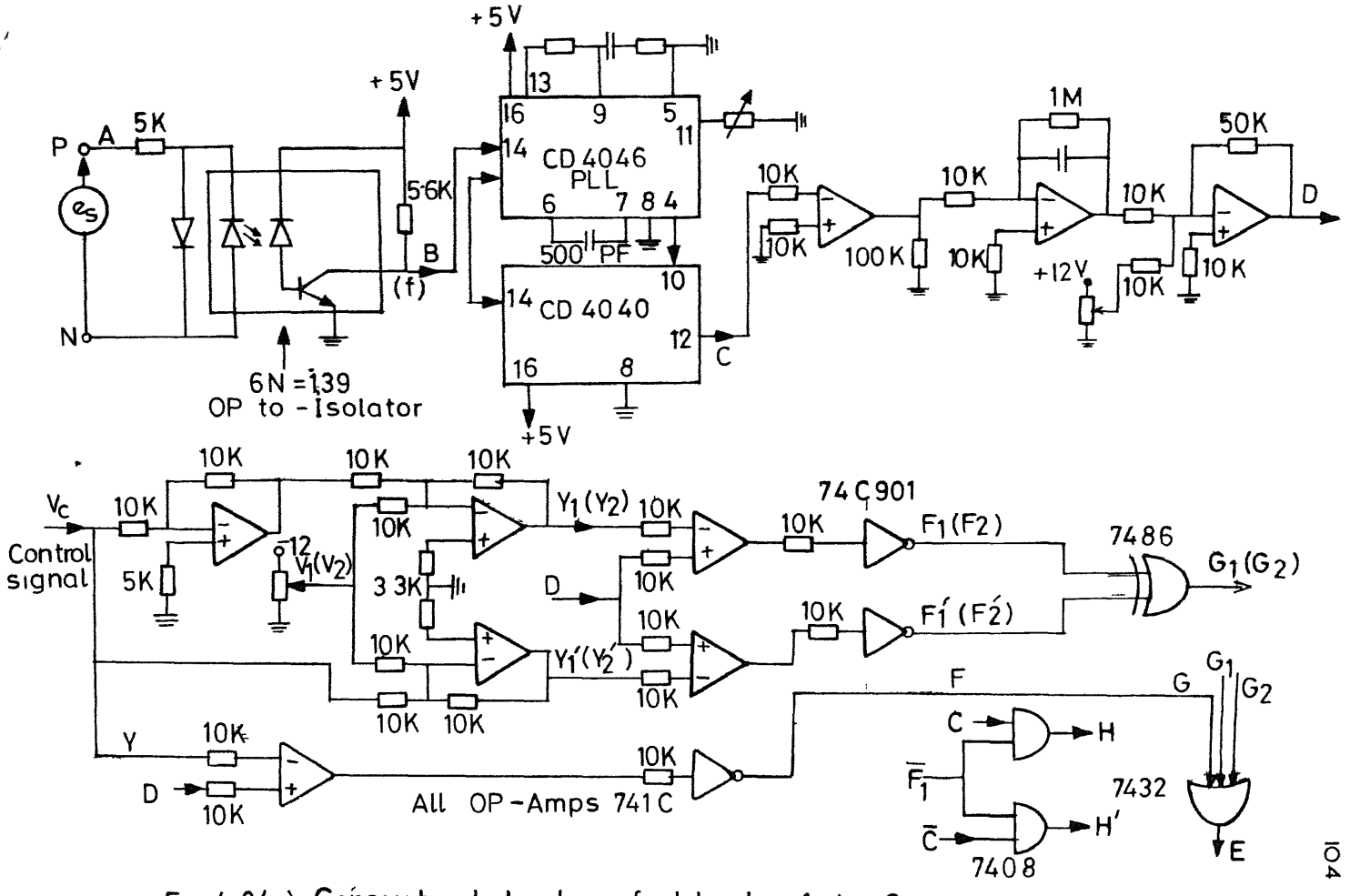


Fig 4·8(a) Circuit details of blocks 1 to 6

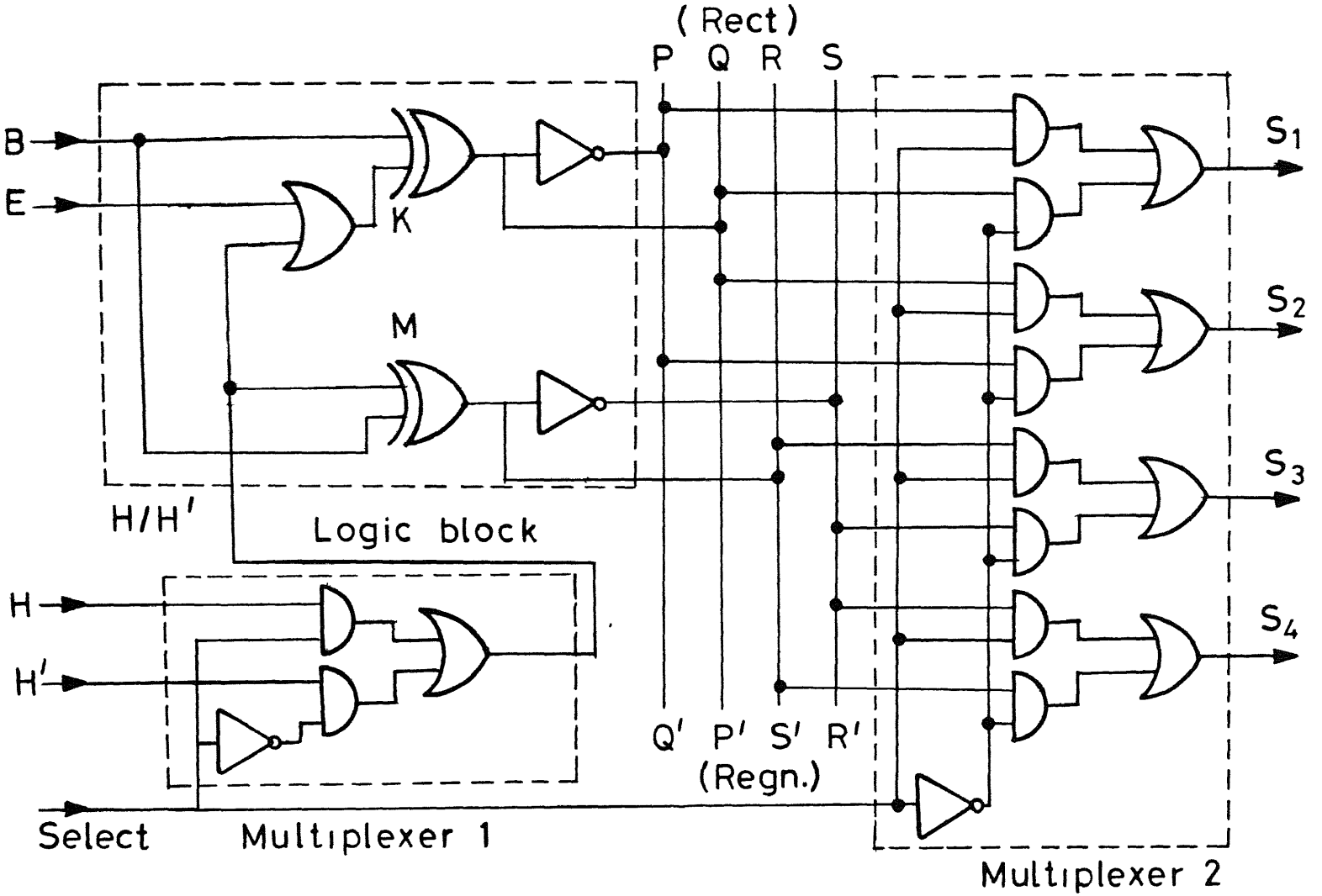


Fig. 4·8(b)Details of the logic blocks 7 to 10 of Fig. 4·6

amplitude A_c. Using op-amps, the control voltage v_c is added to set levels V_1 and V_2 to derive y_1 and y_2 and subtracted from V_1 and V_2 to derive y_1' and y_2'. y_1, y_1', y_2, y_2' and y which is taken as v_c, are compared with the triangular wave D in the different op-amp comparators. The outputs of the comparators are inverted to derive F_1, F_1', F_2, F_2' and F. Using EXCLUSIVE-OR gates the following variables are derived,

$$G_1 = F_1 \oplus F_1'$$

and $$G_2 = F_2 \oplus F_2'$$

E is derived by ORing G_1, G_2 and F.

H and H', which enable the starting of the converter without capacitor precharging, are derived by the following logical operations :

$$H = C.\ \overline{F}_1$$

and $$H' = \overline{C}.\ \overline{F}_1$$

Fig. 4.8(b) shows the details of the logic block and multiplexers 1 and 2 where H, H', B and E derived above are processed to construct the gate pulses. When the 'select' input is high (rectifying mode), the logical expressions of the logic block output are

$$P = \overline{Q}$$

$$Q = B \oplus K$$

$$R = B \oplus H$$

and $$S = \overline{R}$$

where $$K = E + H$$

At the output of the multiplexer 2, P,Q,R,S will appear as S_1, S_2, S_3, S_4 respectively. Similarly, when the 'select' input is low (regenerative mode), the outputs from the logic block are given by

$$P' = B \oplus K$$

$$Q' = \overline{Q}$$

$$R' = \overline{S}$$

$$S' = B \oplus H'$$

where $$K = E + H'$$

And, at the output of the multiplexer-2 P', Q', R', S' will appear as S_1, S_2, S_3, S_4 respectively.

4.7 EXPERIMENTAL VERITIFICATION

Power and control circuits as described earlier were constructed for elimination of maximum three harmonics at a time. The control circuit for three harmonics elimination was employed

Table 4.2

Experimental values (rproposed method)
Load = R-L
I_d = 7A, Load inductance = 100 mH
V_{do} = 198 (= 1 p.u.) for E_{rms} = 220V

rmonic	Converter input			Converter output	p.f.
	E_{rms}	I_{rms}	Power	V_d	
d	230V	2.8A	340W	34V	0.528
	224	4.0	630	76	0.703
	219	4.8	800	110	0.78
	216	5.4	1040	137	0.89
d,5th	227	3.5	455	48	0.57
	221	4.4	660	79	0.68
	220	4.4	835	102	0.86
	218	4.8	900	114	0.86
d,5th,	246	3.7	650	70	0.714
	244	4.4	850	94	0.79
	240	4.9	985	118	0.838

Table 4.3

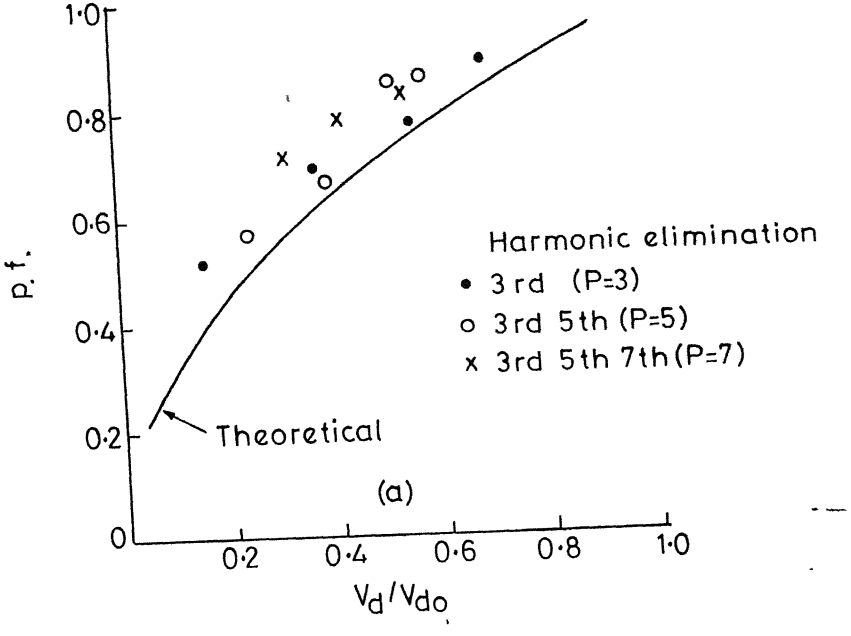
Experimental values : 3rd and 5th harmonics elimination

Load : 3 KW, 220 V dc shunt motor

I_d = 7A, Load inductance = 70 mH

V_{do}(base) = 198 V (= 1 p.u.)

Scheme	Converter input			Converter output		p.f.
	E_{rms}	I_{rms}	Power	V_d	Speed	
Proposed	227V	3.5A	500W	51V	184 rpm	0.63
	222	4.35	695	78.5	370	0.72
	219	4.7	805	94	480	0.78
	211	5.85	1075	143	777	0.87
Alternative	220	3.8	525	56	210	0.63
	217	4.1	600	67	272	0.67
	216	4.4	675	72	357	0.72
	213	5.2	880	106	534	0.79



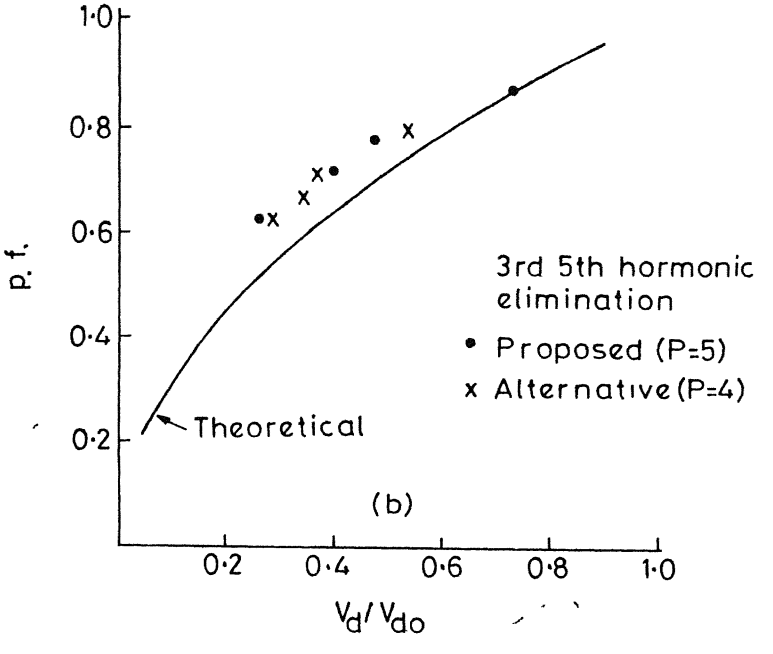


Fig. 4·9 Variation of power factor
(a) R-L Load
(b) Motor Load

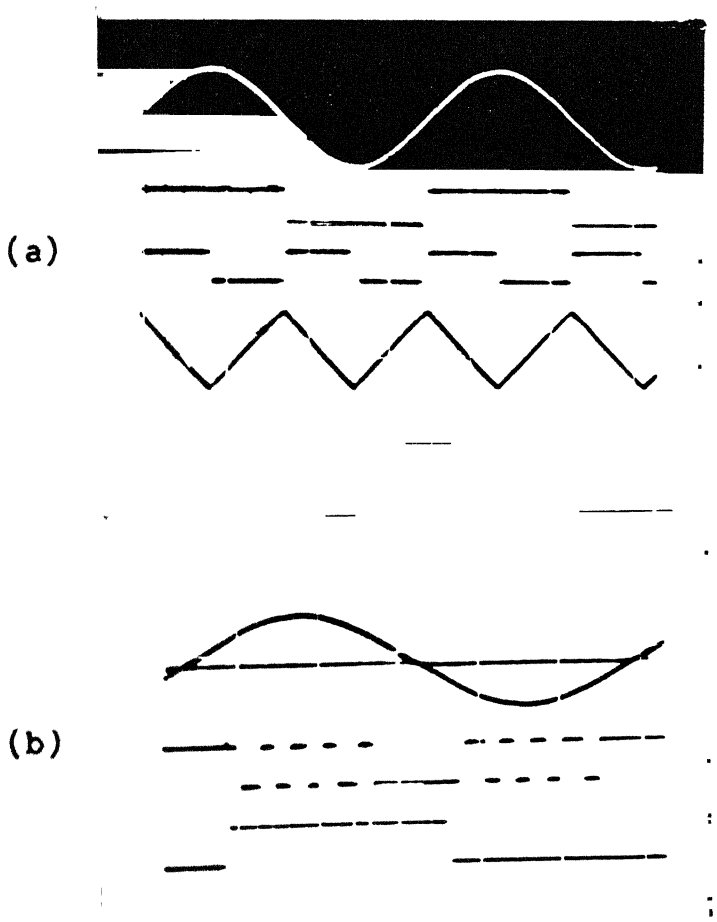


Fig. 4.10 Oscillograms of control circuit waveforms for 3rd and 5th harmonics elimination (rectification mode)
(a) Waveforms A,B,C and D
(b) Waveforms A,S_1 and S_3

(a)

(b)

(c)

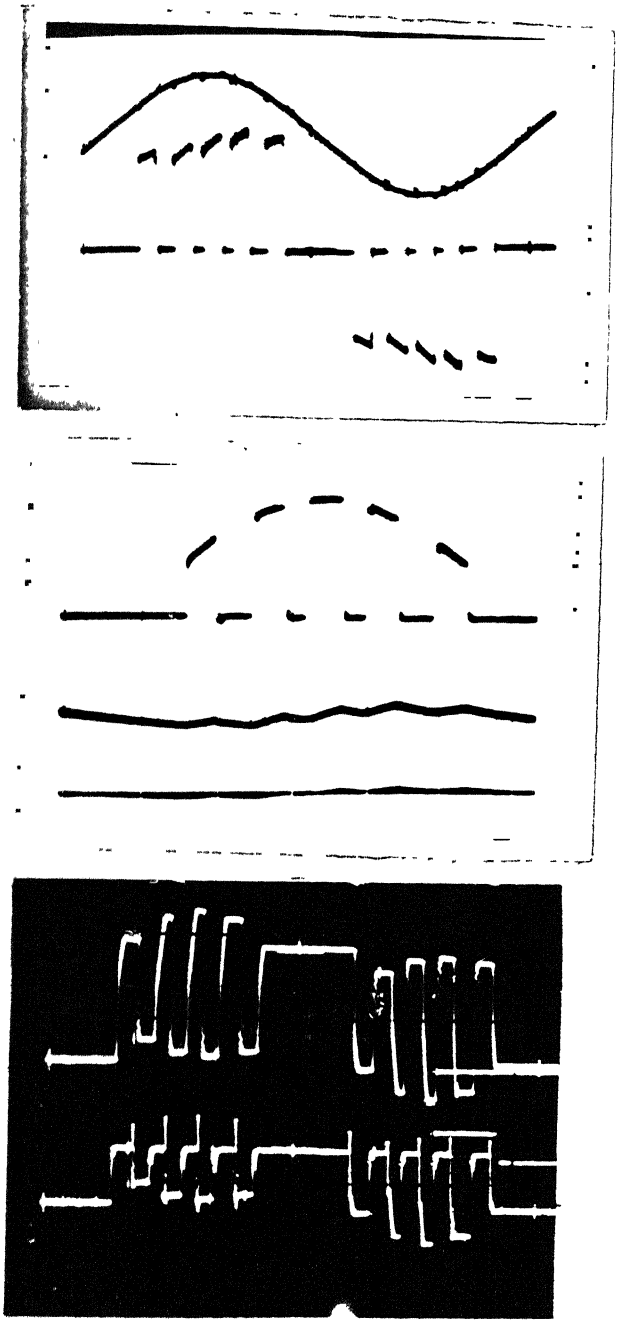


Fig. 4.11 Oscillograms for 3rd and 5th harmonics elimination(rectification)
(a) Line voltage and line current waveforms
(b) Converter output voltage and motor current
(c) Top - Commutating capacitor voltage w.r. to anode of thyristor S_1
Bottom - Anode to cathode voltage of S_1

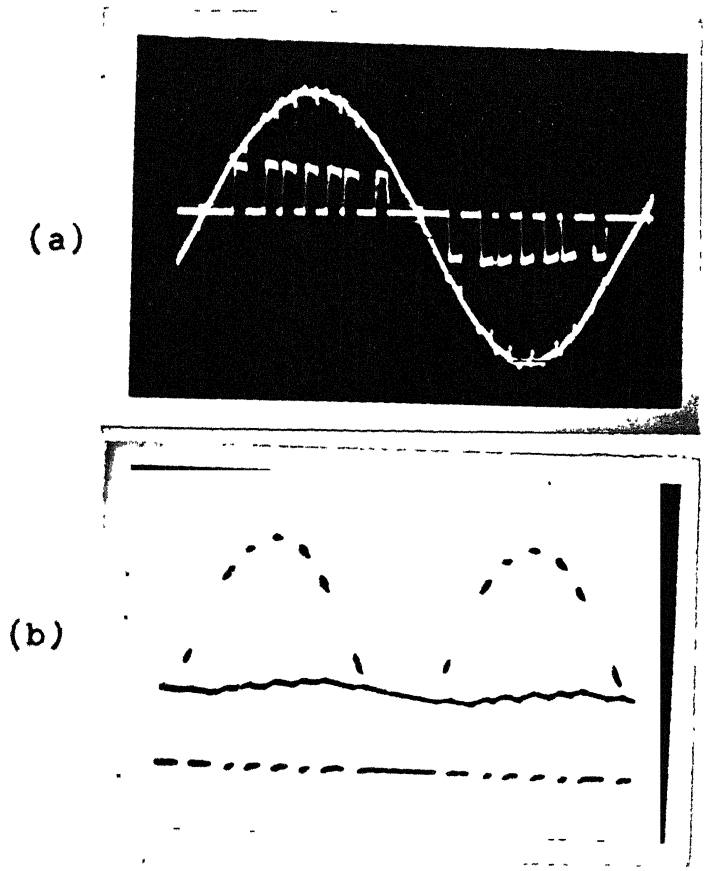


Fig. 4.12 Oscillograms for 3rd, 5th and 7th harmonics elimination (rectification)
(a) Line voltage and line current waveforms
(b) Converter output voltage and the armature current of the motor

for single harmonic and two harmonics elimination also by dropping appropriate number of control pulses. Converter was supplied from 230V, 50Hz supply, and its output voltage, applied to R-L and motor loads, was controlled by harmonic elimination methods.

Tables 4.2 and 4.3 show the measured values of input and output to the converter and calculated power factor in R-L and motor loads respectively. Fig. 4.9 shows that the variation of experimentally observed power factor in the different schemes is in agreement with the theoretical one. Figs. 4.10 through 4.13 show the oscillograms of different waveforms.

4.8 CONCLUSIONS

A selective harmonic eliminating method employing odd number of pulses is presented. Comparison with the method employing even number of pulses shows that the use of odd number of pulses results in better converter performance. It has been shown that owing to fixed pulse positions and equal pulse widths the realisation of the control scheme is fairly simple. Eliminating first few line harmonics by such method would result in reduction in filter cost and filter losses.

CHAPTER 5

COMPARATIVE EVALUATION OF AC CONTROLLER CONTROL SCHEMES

5.1 INTRODUCTION

AC thyristor controllers are widely employed for power control of heating appliances. As mentioned in Chapter 1, the phase-control of ac controllers gives rise to high lower order line current harmonics and low fundamental power factor. Use of external filters for harmonic reduction will require large size filters for filtering of lower order harmonics. This will not only increase the cost of the system but also reduce the system efficiency due to increased losses in the filter circuits. In this context it is desirable to operate the controller with a scheme which results in low lower order harmonics. Based on line- and forced-commutation, several methods have been reported in the literature [27-31] to improve the ac controller performance. Although, the forced-commutation schemes are complex they have the advantages of unity displacement factor and shift of harmonic spectrum to higher order.

In order to find the relative merits of different control schemes, it is necessary to make a comparative study of them for their influence on power factor and harmonic currents. This chapter presents a detailed comparative evaluation of control schemes for single-phase ac controllers.

5.2 CONTROL SCHEMES FOR COMPARISON

The following control schemes for maximum of two forced-commutations per half cycle are considered for comparison.

a. Single stage control

1. Phase control
2. Extinction angle control
3. Extinction angle control with two pulses per half cycle
4. Single-pulse symmetrical pulse-width modulation (SPWM)
5. Two-pulse SPWM
6. Two-pulse sinusoidal PWM

b. Two stage control

This includes the schemes 1 - 5 under single stage control.

The line current waveforms, when the resistive load is controlled by the above schemes, are shown in Fig. 5.1.

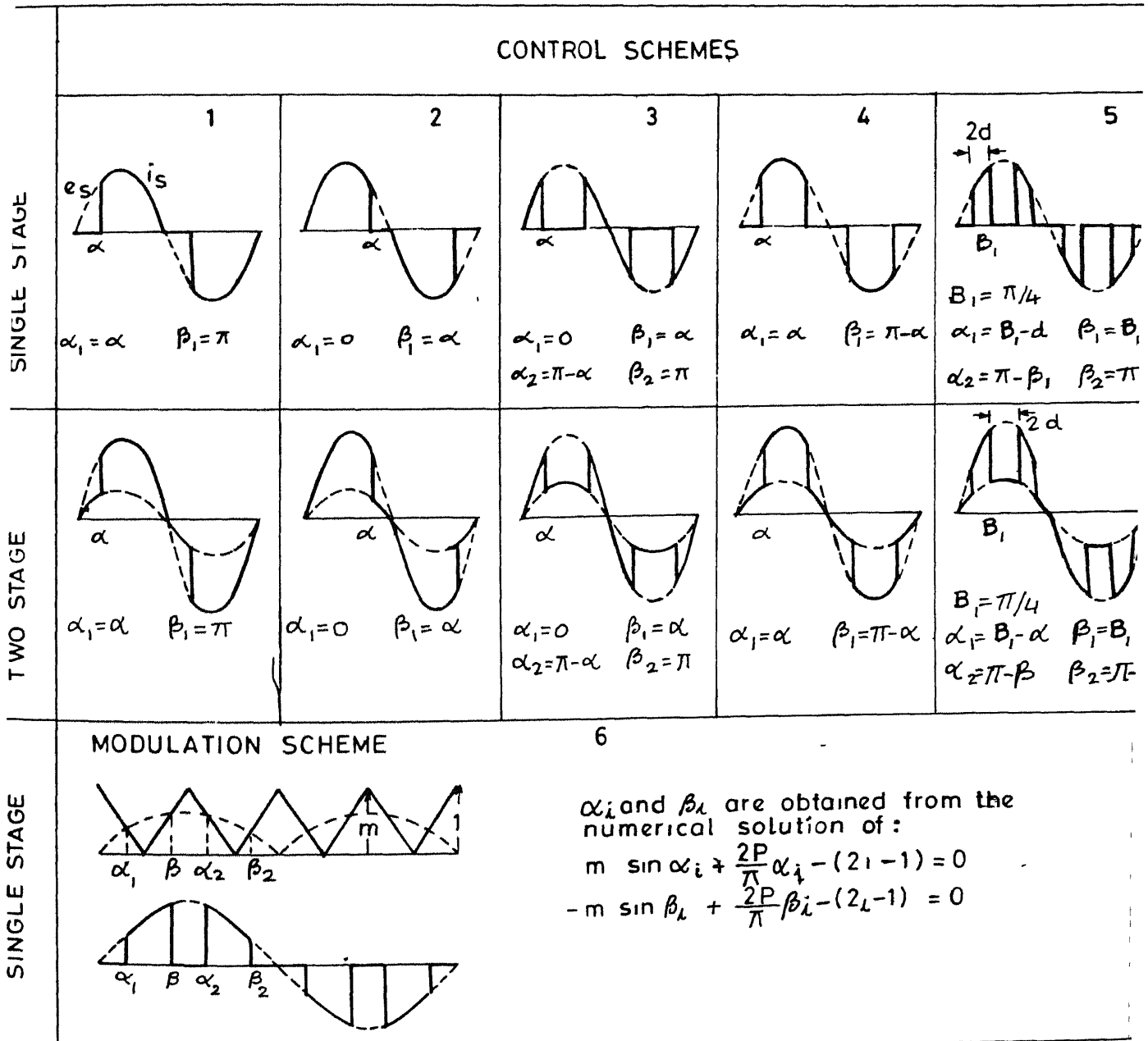
5.3 OPERATING PRINCIPLES

In the following, line- and forced-commutation control of single- and two-stage ac controllers are described. From this general discussion, the operation of an individual scheme under consideration should be quite evident.

5.3.1 Line Commutated ac Controllers

(i) Single stage control

Fig. 5.2(a) shows the power circuit. In the alternate half-cycles, the thyristors S_1 and S_2, when forward biased, are



α_i and β_i are obtained from the numerical solution of:

$$m \sin\alpha_i + \frac{2P}{\pi}\alpha_i - (2i-1) = 0$$

$$-m \sin\beta_i + \frac{2P}{\pi}\beta_i - (2i-1) = 0$$

FIG. 5.1 LINE CURRENT WAVEFORMS WITH DIFFERENT CONTROL SCHEMES FOR R LOAD

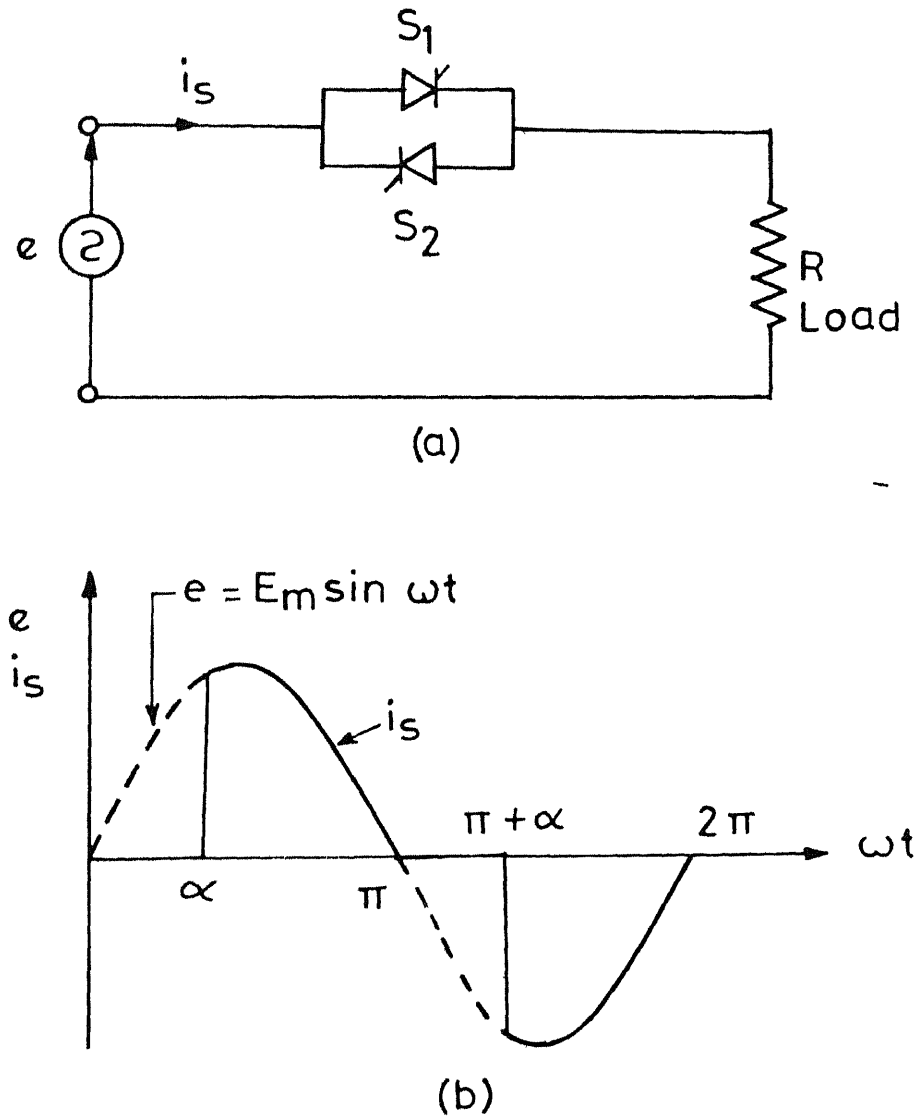


Fig.5·2 (a) Single stage ac controller (line commutation)

(b) Line current waveform

turned on at angle α. Their turn off is natural when the current through them goes to zero. Fig. 5.2(b) shows the resulting line current waveform.

(ii) Two stage control

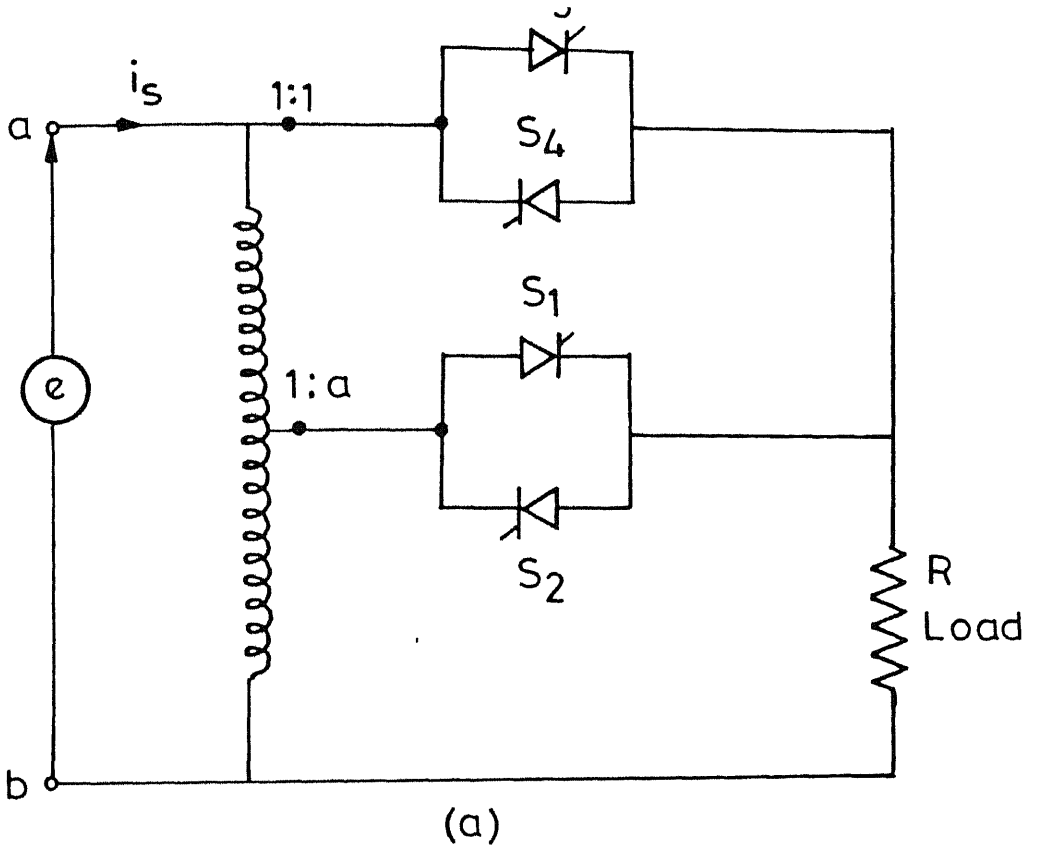
Fig. 5.3(a) shows the power circuit. The load is controlled in the following manner.

For power less than a^2 p.u. ($\frac{I_m^2 R}{2}$ = 1 p.u.), where 'a' is the tap ratio, load is controlled from the lower tap by operating thyristors S_1 and S_2 as in single stage control. For power in the range a^2 to 1 p.u., in the positive half cycle S_1 is turned on at $\omega t = 0$ and S_3 is turned on at $\omega t = \alpha$ which in turn turns off S_1. At $\omega t = \pi$, S_1 turns off naturally due to zero load current. In the negative half cycle, S_2 and S_4 are operated similarly. Fig. 5.3(b) shows the line current waveform.

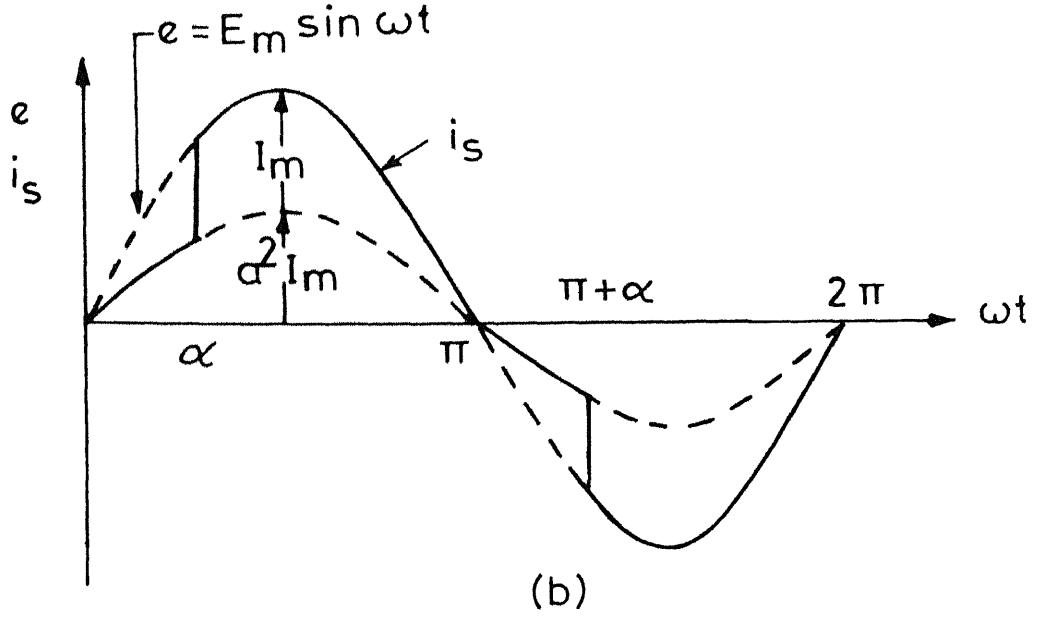
5.3.2 Forced Commutated ac Controllers

(i) Single stage control

Fig. 5.4(a) shows the power circuit [18] for realisation of two forced commutations per half cycle. The pairs of auxiliary thyristors (S_{A1}, S_{A2}) and (S_{A3}, S_{A4}) respectively force commutate the main thyristors S_1 and S_2. Diodes prevent the capacitors from discharging in the reverse direction. In general, for P number of forced commutation per half cycle, the circuit will require commutating elements each of 2P number.



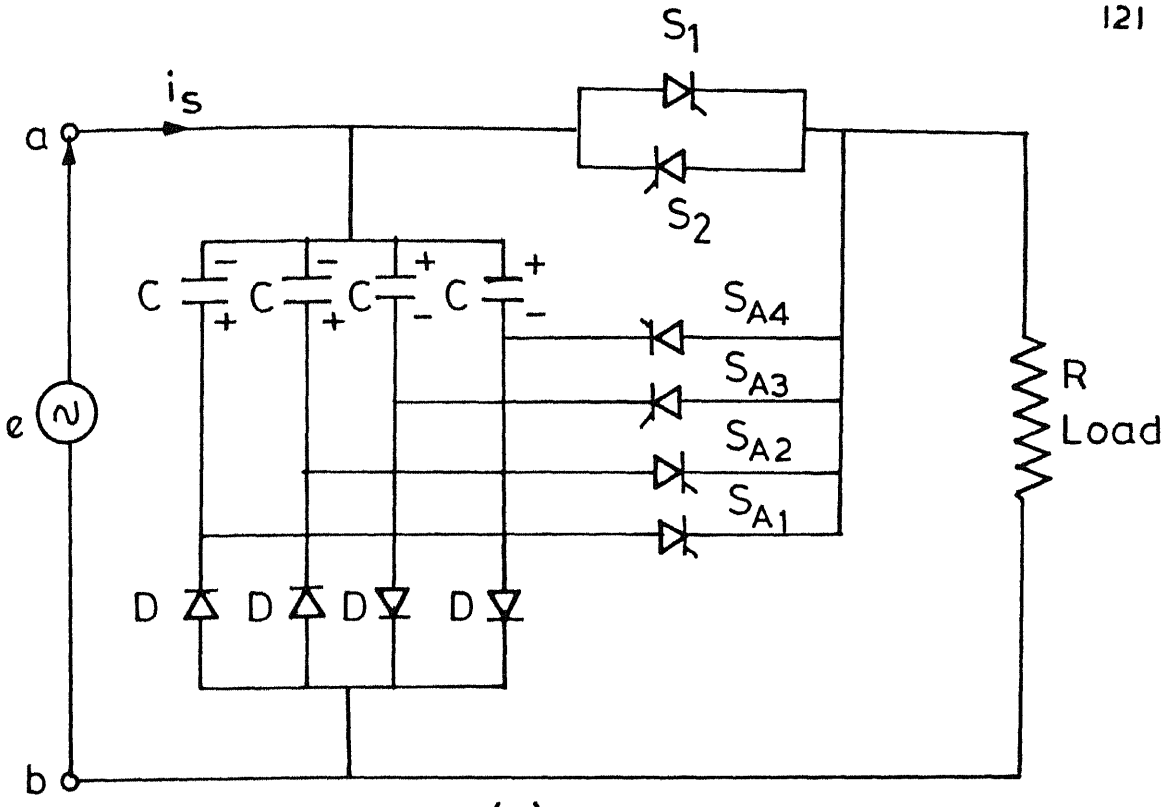
(a)



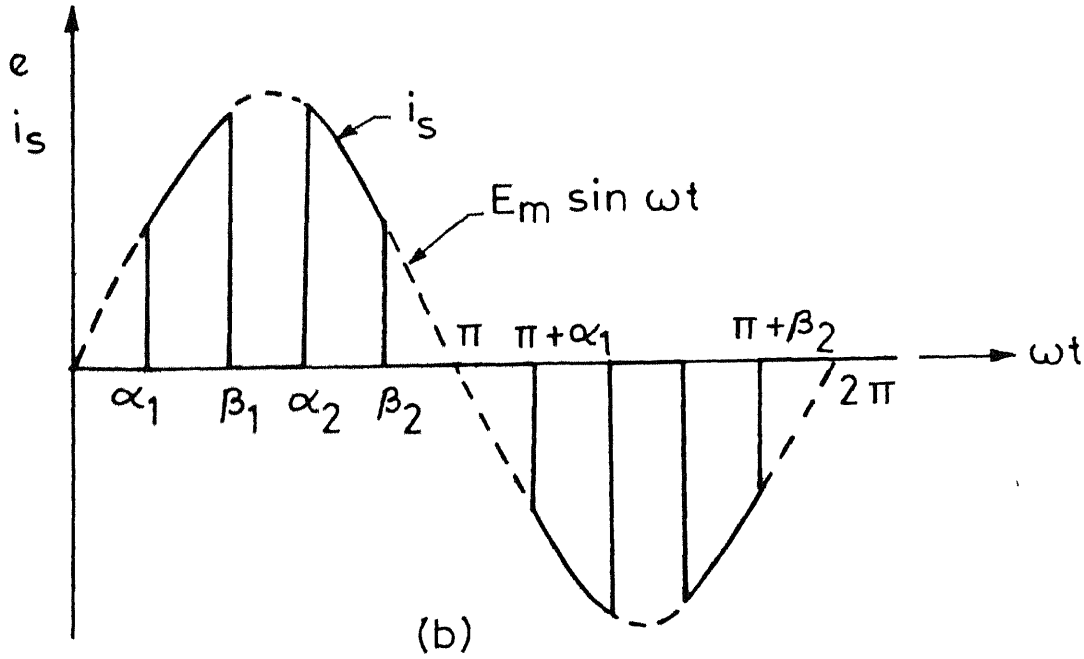
(b)

Fig. 5·3 (a) Two stage controller (line commutation)

(b) Line current waveform



(a)



(b)

Fig. 5·4 (a) Single stage controller (Forced commutation)

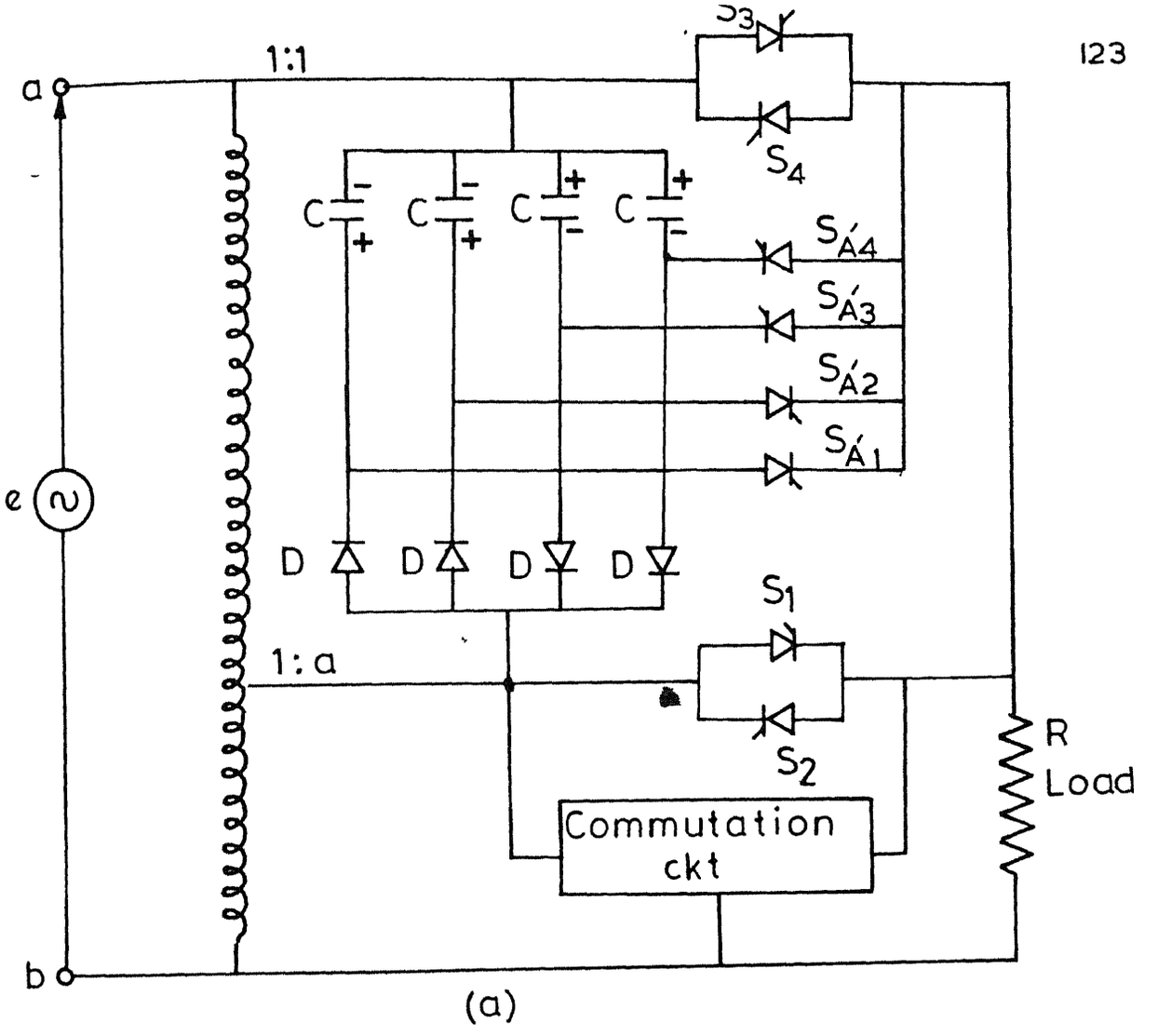
(b) Line current waveform

To explain the circuit operation, let the initial voltage on the capacitors due to previous charging be E_m of polarity as shown in the figure. In the positive half-cycle, when the line terminal 'a' goes positive, S_1 is turned on at α_1 to connect the load to the supply. S_{A1} is triggered at β_1, which turns off S_1 by reverse biasing it with the capacitor voltage. Turning off of S_{A1} is natural. At α_2, S_1 is turned on again at α_2, and is turned off at β_2 by triggering S_{A2}. In the negative half-cycle, thyristors S_2, S_{A3} and S_{A4} are operated similarly. Fig. 5.4(b) shows the resulting line current waveform.

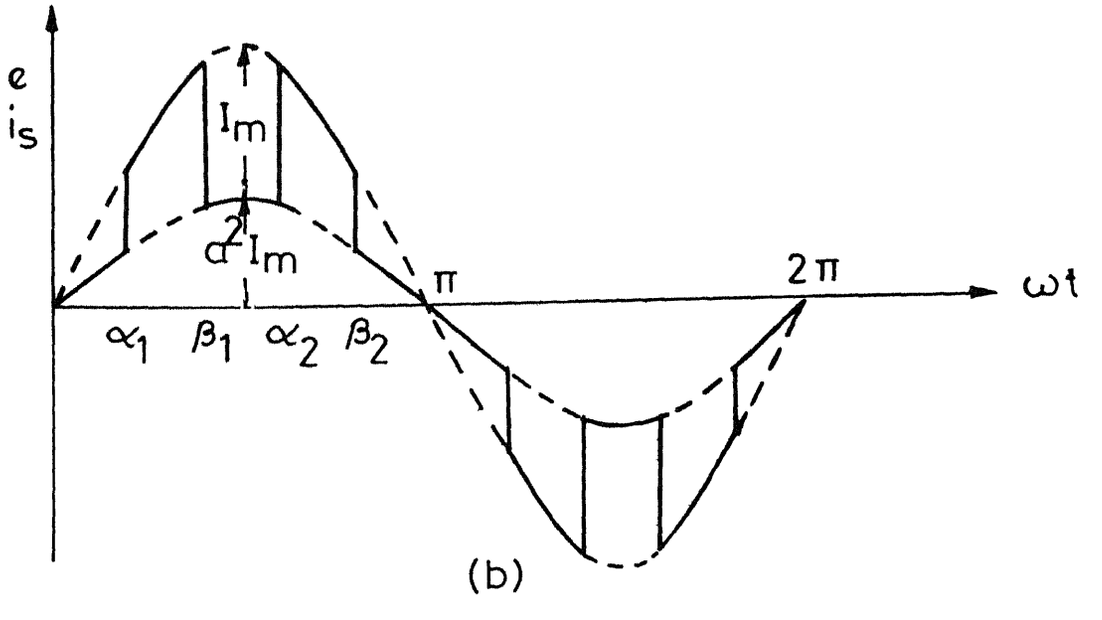
(ii) Two stage control

In Fig. 5.5(a), for power less than a^2 p.u. load is controlled from the lower tap by operating the corresponding thyristors in a sequence stated in the single stage control.

For power higher than a^2, power is controlled by controlling the thyristors of the upper tap. When 'a' goes positive with respect to 'b', the sequence of turning on and turning off of the thyristors is as follows : S_1 is turned on at $\omega t = 0$, β_1



(a)



(b)

Fig 5·5(a) Two stage controller
(Forced commutation)

(b) Line current waveform

and β_2, which connects the load to the lower tap. S_3 is turned on at $\omega t = \alpha_1$ and α_2, which turns off S_1 by reverse biasing S_1 and connects the load to the upper tap. S_3 is turned off by firing S'_{A1} and S'_{A2} at β_1 and β_2 respectively. When 'a' goes negative with respect to 'b' S_2, S_4, S'_{A3} and A'_{A4} are operated similarly. Fig. 5.5(b) shows the resulting line current waveform.

5.3.3 Analysis

The generalised harmonic coefficients for a two stage controller with P pulses per half cycle are derived as follows.

a. Load less than a^2 p.u.

In Fig.5.5(b), the line current i_s is given by

$$i_s = a^2 \sin\omega t \qquad (5.1)$$

where

$$\alpha_i \leq \omega t \leq \beta_i \qquad (5.2)$$

$$i = 1,2, \ldots, P .$$

Since, $i_s(\omega t) = -i_s(\omega t+\pi)$, from the Fourier analysis of eqns. (5.1) and (5.2) the harmonic coefficients may be derived as

$$a_1 = -\frac{a^2}{2\pi} \sum_{i=1}^{P} (\cos 2\beta_i - \cos 2\alpha_i) \qquad (5.3)$$

$$b_1 = \frac{a^2}{2\pi} \sum_{i=1}^{P} (2\beta_i - 2\alpha_i - \sin 2\beta_i + \sin 2\alpha_i) \qquad (5.4)$$

$$a_n = a^2 x$$

$$b_n = a^2 y$$

where

$$x = \frac{1}{\pi} \sum_{i=1}^{P} \left[\frac{\cos N_1\alpha_i - \cos N_1\beta_i}{N_1} - \frac{\cos N_2\alpha_i - \cos N_2\beta_1}{N_2}\right] \qquad (5.5)$$

$$y = \frac{1}{\pi} \sum_{1=1}^{P} \left[\frac{\sin N_1\alpha_i - \sin N_1\beta_i}{N_1} - \frac{\cos N_2\alpha_i - \cos N_2\beta_1}{N_2}\right] \qquad (5.6)$$

$N_1 = n + 1$

$N_2 = n - 1$

and n = harmonic order

$= 3,5,7, \ldots,$

The rms value of the line current is given by

$$I_{rms} = \left[\frac{1}{\pi} \sum_{i=1}^{P} \int_{\alpha_i}^{\beta_i} i_s^2 \, d\omega t\right]^{1/2}$$

$$= \frac{a^2}{2} \left[\frac{1}{\pi} \sum_{i=1}^{P} (2\beta_i - 2\alpha_i - \sin 2\beta_i + \sin 2\alpha_i)\right]^{1/2} \qquad (5.7)$$

b, Load greater than a^2

For power between a^2 and 1, from Fig. 5.5(b), the line current may be written as

$$i_s = i_{s1} + i_{s2}$$

where $i_{s1} = a^2 \sin\omega t$ for $0 \leq \omega t < \pi$ (5.8)

and $i_{s2} = (1-a^2)\sin\omega t$ for $\alpha_i < \omega t < \beta_i$; $i = 1$ to P (5.9)

From eqns. (5.8) and (5.9), the rms line current is given by

$$I_{rms} = \left[\frac{1}{\pi} \sum_{i=1}^{P+1} \int_{\beta_{i\,1}}^{\alpha_i} i_{s1}^2 \, d\omega t + \frac{1}{\pi} \sum_{1=1}^{P} i_s^2 \, d\omega t\right]^{1/2}$$

$$= \frac{1}{2} (a^2 A + B)^{1/2} \qquad (5.10)$$

where $A = \frac{a^2}{\pi} \sum_{i=1}^{P+1} (2\beta_{i-1} - 2\alpha_i - \sin 2\beta_{1-1} + \sin 2\alpha_i)$

$$B = \frac{1}{\pi} \sum_{1=1}^{P} (2\beta_1 - 2\alpha_i - \sin 2\beta_i + \sin 2\alpha_i)$$

$$\beta_o = 0$$

and $\alpha_{P+1} = \pi$.

Line harmonics are due to the component i_{s2}. Hence from eqn. (5.9), the harmonic coefficients are given by

$$a_1 = -\frac{(1-a)^2)}{2\pi} \sum_{i=1}^{P} (\cos 2\beta_i - \cos 2\alpha_i) \qquad (5.10)$$

$$b_1 = a^2 + \frac{(1-a^2)}{2\pi} \sum_{i=1}^{P} (2\beta_i - 2\alpha_i - \sin 2\beta_i + \sin 2\alpha_1) \qquad (5.11)$$

$$a_n = x(1-a^2) \qquad (5.12)$$

$$b_n = y(1-a^2) \qquad (5.13)$$

where x and y have the same values as given in eqns. (5.5) - (5.6).

With a = 1 eqns. (5.3) - (5.7) in general hold good for single stage control. The values of α and β for the different schemes are stated in Fig. 5.1. Different performance criteria are given below.

rms harmonic current, $I_n = (\frac{a_n^2 + b_n^2}{2})^{1/2}$

Fundamental power factor, FPF = $\cos(\tan^{-1} \frac{a_1}{b_1})$

Distortion factor, DF = I_1/I_{rms}

Total power factor, p.f. = FPF. DF

5.4 COMPARATIVE PERFORMANCE

Figs. 5.6 - 5.8 show the relative variation of different quantities while single stage controllers and two stage controllers with tap ratio a = 0.5 are operated with different control schemes for improvement of line condition. The numerals on the graphs correspond the order of the schemes.

a. Single stage control

Fundamental Power Factor :

(i) Schemes 3 - 6 have fundamental p.f. unity and hence external reactive power compensators are not required.

(ii) In schemes 1 and 2, the fundamental p.f. has same value except that it is leading in the latter one. For FPF to be unity, schemes 1 and 2 will need leading and lagging compensation respectively.

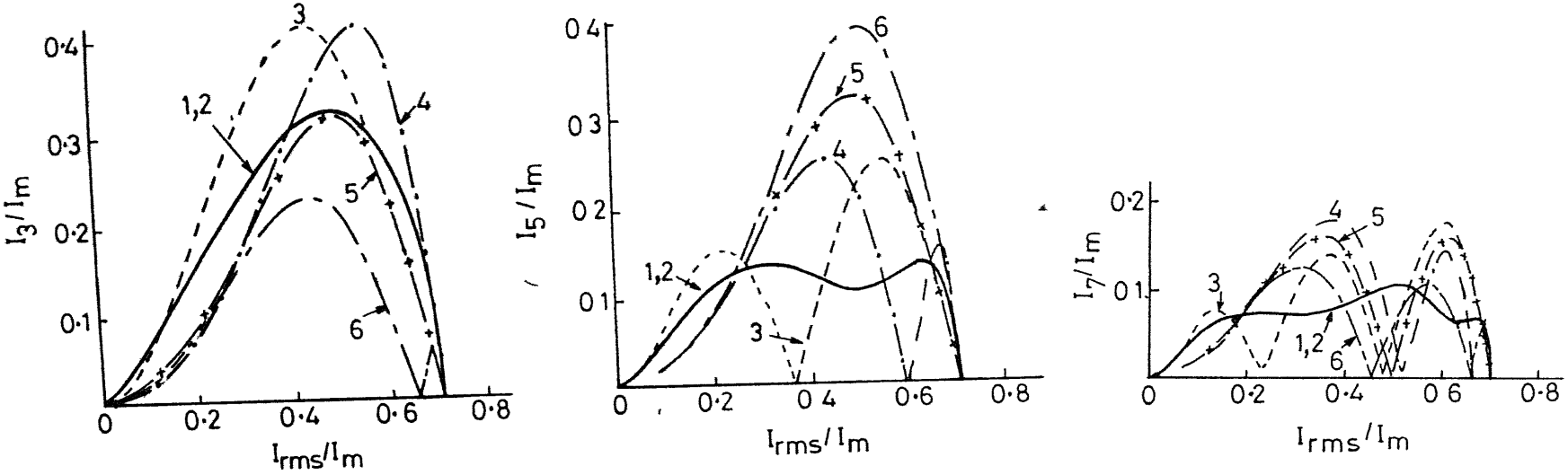


Fig.5·6 Variation of line current harmonics with rms line current in different control schemes of single phase ac-controller with R load

Single stage control

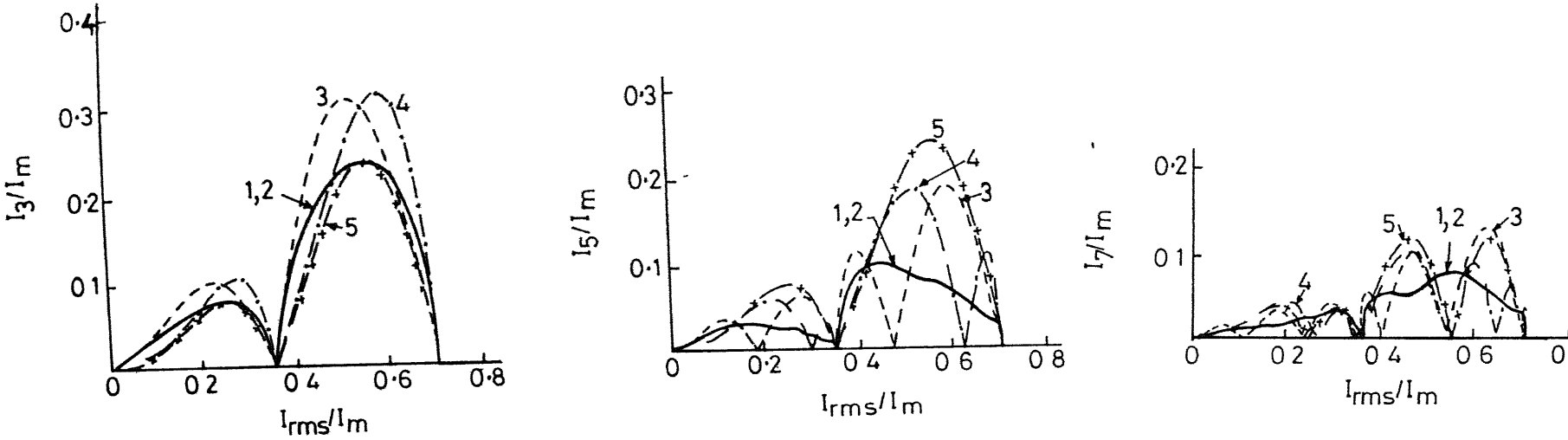


Fig 5 7 Variation of line current harmonics with rms line current in different control schemes of single phase ac-controller with R load

Two stage control

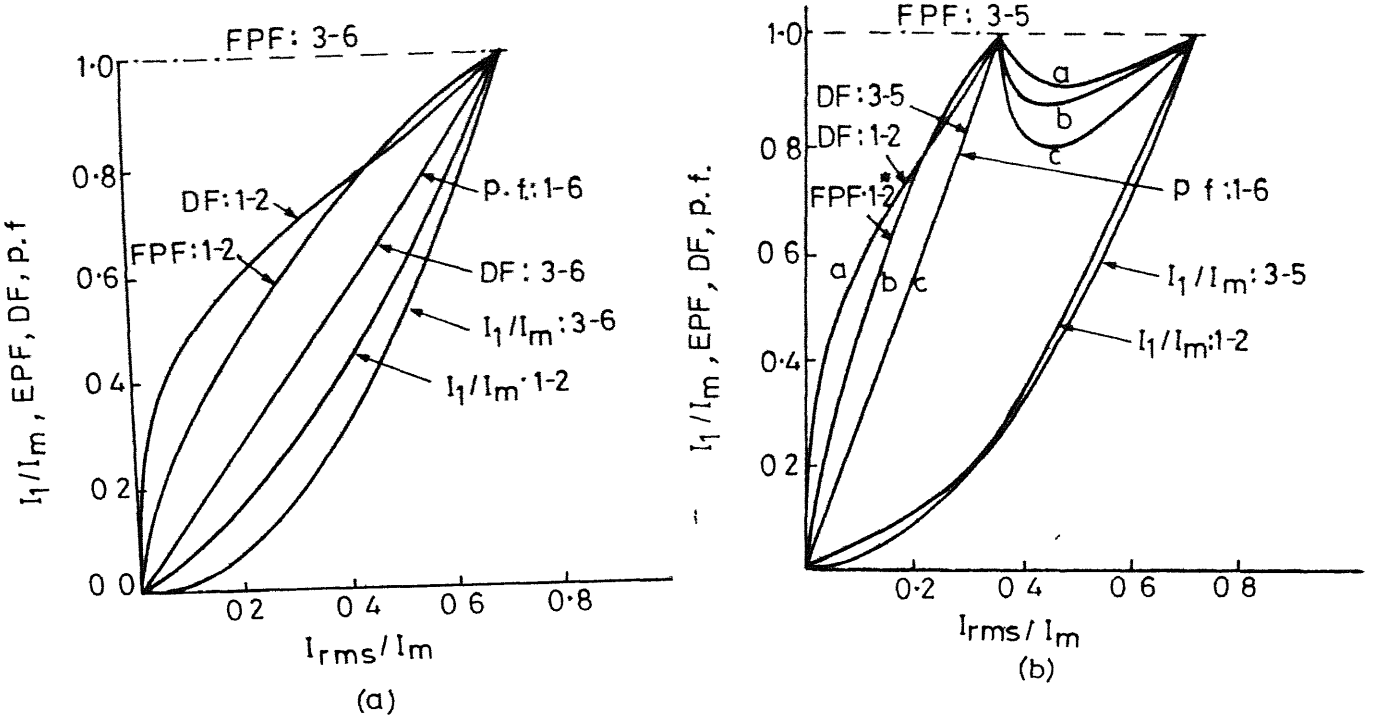


Fig 5.8 Variation of fundamental power factor (FPF) distortion factor (DF), total power factor (pf) and fundamental line current with rms line current in different control schemes of single phase ac controller with R load

(a) Single stage control

(b) Two stage control

Distortion Factor :

Distortion factor in schemes 1 and 2 has the same value. Similarly it has the same value in schemes 3-6. Due to lower value of DF, the total harmonic content in the line current in schemes 3-6 is higher than that of schemes 1-2. However, the cost of the filter circuits in the individual scheme will mostly be determined by first few predominant lower order harmonics.

Total Power Factor :

Line power factor in all the schemes, whether line - or forced - commutated, is the same. Thus, in the pulsewidth modulation schemes, where the distortion factor and the line power factor are the same, attempt of reducing lower order, harmonics will tend to increase the higher order harmonics. Although, the filtering of higher order harmonics is simple .

Line Current Harmonics :

(i) As the filter size is decided by lowest order harmonics, scheme 6 is the best due to the lowest 3rd harmonic. Through, the schemes 1-2 and 5 have peak 3rd harmonic content same, schemes 1-2 are better than 5 due to lower 5th harmonic content in the former ones. Schemes 3 and 4 are the worst due to highest 3rd harmonic content. This also holds good for three-phase star-connected load with star point connected to neutral. In this case, line will carry all the harmonics and the neutral will carry in-phase triplen harmonics.

(ii) In the case of three-phase delta connected load, with thyristor switches in series of each phase of the load, line current will be free from the triplen harmonics. In this case, 5th harmonic will be of primary concern in determining the filter size. In this context, considering the peak amplitudes of 5th and 7th harmonic components, schemes 1-2 are the best followed by 3,4,5 and 6 in order of preference.

b. Two Stage Control

In two stage control, distortion factor and line power factor are much improved over single stage control. With more number of stages harmonic content can be reduced to a very small value and power factor may be maintained near to unity over a wide range of control.

Improvement over single stage control depends upon the choice of tap ratio, a. For minimization of harmonic amplitudes, tap-ratio 'a' should be such that, in Fig. 5.7(b), the peak harmonic current in the range $0 < I_{rms}/I_m < \frac{a^2}{\sqrt{2}}$ becomes equal to the peak harmonic current in the range $\frac{a^2}{\sqrt{2}} < I_{rms}/I_m < 1/\sqrt{2}$. As the ratio of these currents is $a^2/(1-a^2)$, this gives optimum tap ratio as, $a = 0.707$. For example, in schemes 1-5, the peak amplitudes of 3rd harmonic

current with a = 0.5 are 25%, 25%, 32%, 32% and 25% respectively whereas with a = 0.707 the corresponding values are 16.6%, 16.6%, 21%, 21% and 16.6%.

5.5 CONCLUSIONS

In this chapter, a comparative study of different control schemes of ac controllers with resistive load is carried out. It is believed that the result presented here will be useful in selecting a proper control scheme.

CHAPTER 6

ELIMINATION OF LINE CURRENT HARMONICS IN AC CONTROLLERS FEEDING A RESISTIVE LOAD

6.1 INTRODUCTION

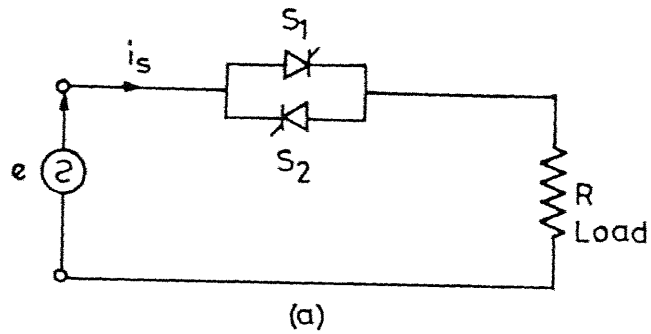
AC phase controllers suffer from the drawback of low power factor and generation of line current harmonics which cause disturbance to other equipments operating on the same line. Some applications require that certain harmonics be eliminated or reduced. For example, in utility systems, the triplen harmonics, which are in phase and flow through neutral wire, need to be reduced to reduce the loading of the neutral wire. Similarly, in the applications like carrier-current protections in the power systems, it is desirable to eliminate those harmonics which fall near the signal frequency for proper functioning of protection systems. As it is easier to filter out higher order harmonics, lower order harmonics deserve more attention. Bland [29] has attempted to eliminate any one line harmonic at a time. In this the relation between firing and extinction angles is derived by equating the harmonic coefficient to zero. Power variation is obtained by variation of firing and extinction angles. However, their relationship is nonlinear, and the implementation is difficult. Krishnamurthy et al. [30-31] have suggested two methods ; one,

for reduction of single line harmonic at a time and other, for elimination of two or more harmonics. Both the methods assumes even number of pulses per half cycle which are located at fixed positions, and the power variation is obtained by varying the pulse widths symmetrically around the pulse positions.

In this chapter, pulse width modulation techniques employing odd number of pulses per half cycle are considered. Two methods are presented for harmonic control : reduction of a single harmonic at a time, and elimination of two or more harmonics at a time. In both the methods, the pulses are located at fixed positions and the power control is affected by varying the pulse widths symmetrically around the pulse positions. Present methods are compared with the alternative methods[30-31] for their performance. Power circuit to implement the above methods is presented.

6.2 GENERALISED METHOD OF SELECTIVE HARMONIC ELIMINATION

Figure 6.1(a) represents an ac controller feeding a resistive load. When line 'a' goes positive, S_1 is turned on at α_1 and turned off at β_1. It is again turned on at α_2 and turned off at β_2. Such operations are repeated P times at different time instants during the positive half cycle. In the negative half cycle when line 'b' goes positive, S_2 is operated similarly. The line current and line voltage waveforms are as shown in Fig. 6.1(b). In order to keep the



(a)

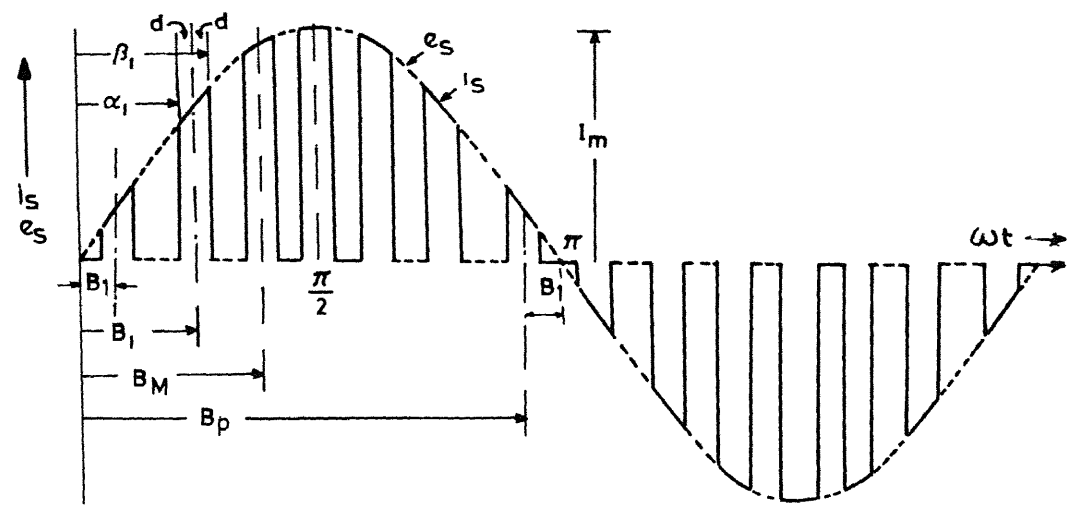


Fig. 6·1(b) Lime voltage/current wavefrom for resistive load

fundamental power factor unity, the P pulses of the load current, each of width 2d, are placed symmetrically about the $\pi/2$ axis. In a PWM scheme consisting of P number of pulses/ half cycle, either even or odd in value, the pulse positions $B_1, B_2, \ldots, B_p$ are related as follows :

$$P \text{ odd number : } P = 2M + 1, \tag{6.1}$$

$$B_{P+1-i} = \pi - B_i \qquad i = 1,2, \ldots, M$$
$$\text{and } B_{M+1} = \pi/2 \tag{6.2}$$

$$P \text{ even number : } P = 2M,$$
$$\text{and } B_{P+1-i} = \pi - B_i \qquad i = 1,2, \ldots, M$$

Turn on and turn off angles are given by

$$\alpha_i = B_i - d, \tag{6.3}$$
$$\text{and } \beta_i = B_i + d, \qquad i = 1,2, \ldots, P$$

From the Fourier analysis, the harmonic coefficients, normalized with respect to peak load current I_m ($= E_m/R$), are given by

$$a_1 = 0$$
$$b_1 = \frac{2}{\pi}\left[d.P - \sin 2d\left(\sum_{i=1}^{M} \cos 2B_i - \frac{K}{2}\right)\right] \tag{6.4}$$

$$a_n = 0$$
$$\text{and } b_n = A\left[\sum_{i=1}^{M} \cos(n-1)B_i + \frac{K}{2}\cos(n-1)\pi/2\right] \tag{6.5}$$
$$-B\left[\sum_{i=1}^{M} \cos(n+1)B_i + \frac{K}{2}\cos(n+1)\pi/2\right]$$

where $A = \frac{4}{(n-1)\pi} \sin(n-1)d$

$B = \frac{4}{(n+1)\pi} \sin(n+1)d$

$n = 3,5,7, \ldots,$ order of harmonics

and $K = 1$ for P odd

$= 0$ for P even (6.6)

Normalised rms line current

$$I_{rms} = \left[\frac{1}{\pi} \int_0^{\pi} \left(\frac{i_a}{I_m}\right)^2 d\omega t\right]^{1/2}$$

$$= \left[\frac{1}{\pi} \sum_{i=1}^{P} \int_{\alpha_i}^{\beta_i} \sin^2 \omega t \, d\omega t\right]^{1/2}$$

$$= (b_1/2)^{1/2} \qquad (6.7)$$

From the above, the rms fundamental and harmonic currents, and power factor are given by

$$I_1 = b_1/\sqrt{2} = \sqrt{2} \cdot I_{rms}^2 \qquad (6.8)$$

$$I_n = b_n/\sqrt{2} \qquad (6.9)$$

and $$p.f. = \frac{I_1}{I_{rms}} = \sqrt{2}\, I_{rms} \qquad (6.10)$$

Equations (6.8) and (6.10) show that, in the symmetrical PWM schemes, the variation of the fundamental line current and the

line power factor with the rms line current is independent of the number of pulses used per half cycle. Fig. 6.2 shows the variation of power factor and the fundamental current for multi-pulse SPWM schemes.

In the scheme as stated, locating the pulses at the proper positions, any M number of harmonics can be eliminated from the line current. The rules for fixing the pulse positions may be derived by equating the harmonic coefficients of the harmonics to be eliminated to zero. Hence, from eqn. (6.5), the necessary conditions to be satisfied for elimination of M harmonics given by $n = n_1, n_2, \ldots, n_M$ are :

$$\sum_{i=1}^{M} \cos(n-1)B_i + \frac{K}{2} \cos(n-1)\,\pi/2 = 0 \qquad (6.11)$$

subject to the constraints

$$\sum_{i=1}^{M} \cos(n+1)B_i + \frac{K}{2} \cos(n+1)\pi/2 = 0 \qquad (6.12)$$

and

$$B_1 < B_2 < \ldots < B_M < \pi/2 \,. \qquad (6.13)$$

The M transcendental equations given by eqn. (6.11) may be solved for $B_1, B_2, \ldots, B_M$ using numerical methods. Power variation is affected by varying the pulse width around the pulse position symmetrically.

It is shown in the following that out of the two alternatives (use of odd number of pulses or even number of pulses) for

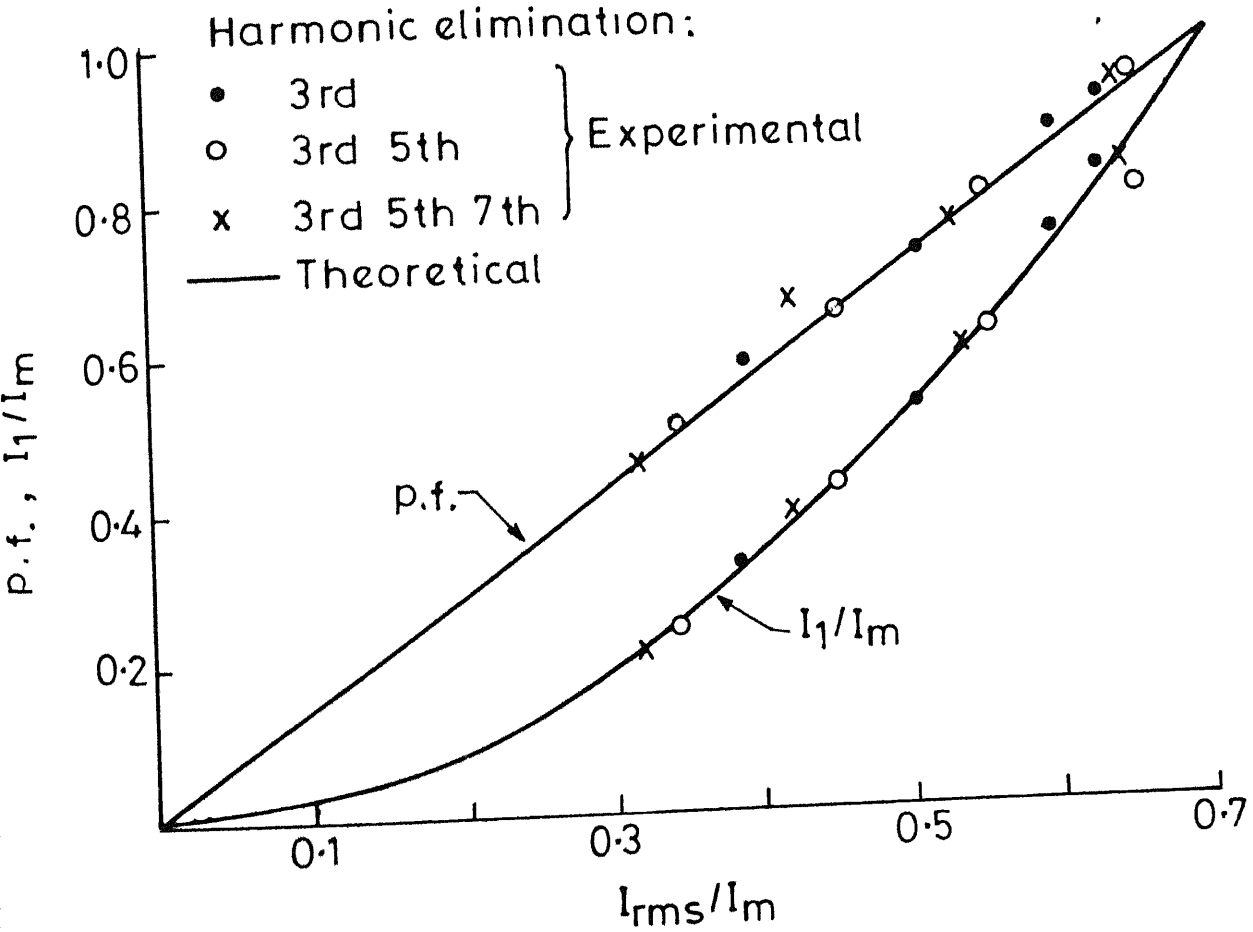


Fig. 6·2 Variation of fundamental current and power factor with rms line current in PWM control schemes with quarter wave symmetry

selective harmonics elimination, the use of odd pulses results into better performance, and therefore, it is proposed to use odd pulses.

6.2.1 Elimination of Two Line Current Harmonics

Consider the elimination of 3rd and 5th harmonics. Hence, M = 2 and n = 3 and 5.

P, odd number : From eqns. (6.11) to (6.13), for K = 1, the equations to be satisfied are :

$$\cos 2B_1 + \cos 2B_2 - 0.5 = 0$$

$$\cos 4B_1 + \cos 4B_2 + 0.5 = 0$$

With the constraints

$$\cos 6B_1 + \cos 6B_2 - 0.5 = 0$$

and $0 < B_1 < B_2 < \pi/2$.

Using Newton-Raphson method, the numerical solution of the above equations is

$$B_1 = 18^\circ \quad \text{and} \quad B_2 = 54^\circ.$$

P, even number : From eqns. (6.11) to (6.13), for K = 0,

$$\cos 2B_1 + \cos 2B_2 = 0$$

$$\cos 4B_1 + \cos 4B_2 = 0$$

with the constraints

$$\cos 6B_1 + \cos 6B_2 = 0$$

and $0 < B_1 < B_2 < \pi/2$.

The solution of the above equations is

$$B_1 = 22.5^\circ \quad \text{and} \quad B_2 = 67.5^\circ \ .$$

Variation of different harmonic components in the above two cases are shown in Fig. 6.3(b).

6.2.2 Elimination of three Line Current Harmonics

Let 3rd, 5th and 7th harmonics are to be eliminated. Hence, M = 3, and n = 3,5 and 7.

P, odd number : As before, following equations may be written :

$$\cos 2B_1 + \cos 2B_2 + \cos 2B_3 - 0.5 = 0$$

$$\cos 4B_1 + \cos 4B_2 + \cos 4B_3 + 0.5 = 0$$

$$\cos 6B_1 + \cos 6B_2 + \cos 6B_2 - 0.5 = 0$$

with the constraints

$$\cos 8B_1 + \cos 8B_2 + \cos 8B_3 + 0.5 = 0$$

and $B_1 < B_2 < B_2 < \pi/2$.

Solution to the above equations is

$$B_1 = 12.85^\circ, \quad B_2 = 38.55^\circ$$

and $B_2 = 64.25^\circ$.

P, even number : For K = 0, the solution of eqns. (6.11) to (6.13) gives

$$B_1 = 15^\circ, \quad B_2 = 45^\circ \quad \text{and} \quad B_3 = 75^\circ \ .$$

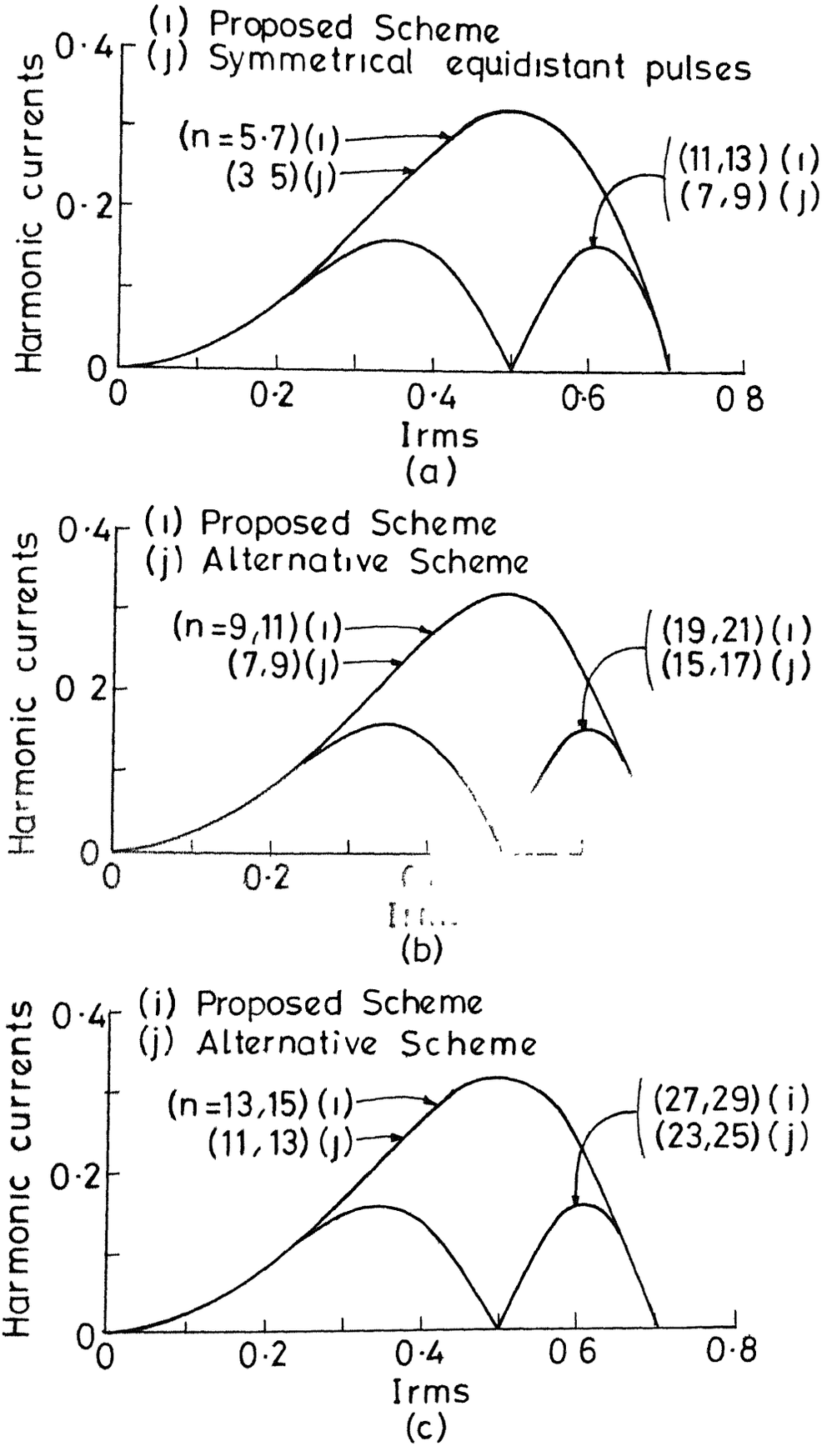


Fig. 6·3 Variation of the normalised peak harmonic currents with normalised rms line current
(a) 3rd harmonic elimination
(b) 3rd and 5th harmonic elimination
(c) 3rd, 5th and 7th harmonics elimination

Fig. 6.3(c) shows the variation of harmonics in the above two cases.

6.2.3 Elimination of Third Harmonic Line Current

Significannce of 3rd harmonic elimination has been stated earlier. In the case of odd pulse width modulation scheme, the equations to be satisfied for 3rd harmonic elimination are :

$$\cos 2B_1 - 0.5 = 0$$

with the constraints

$$\cos 4B_1 + 0.5 = 0$$

and $B_1 < \pi/2$.

The solution to the above equation is

$$B_1 = 30^\circ .$$

The placing of three pulses at 30°,90° and 150°, i.e., equidistant, will eliminate all the triplen harmonic components from the line current. However, the harmonics other than triplen do not result any solution, and hence, cannot be eliminated.

In an alternative scheme which involves two pulses per half cycle, no harmonic satisfies the conditions given in eqns. (6.11) to (6.13). Hence, this scheme is inadequate to eliminate any one harmonic. For comparison with three-pulse scheme, the performance of this scheme is studied with equidistant pulse arrangement.

Fig. 6.3(a) shows the variation of different harmonics in the 2-pulse and 3-pulse schemes in which pulses are located at equidistant.

6.2.4 Comparison of the Proposed and Alternative Methods

From Figs. 6.2 and 6.3 following comparison may be made for the schemes of harmonic elimination, i.e., schemes with odd number of pulses and even number of pulses per half cycle.

1) The variation of p.f. and the fundamental line current are the same in both the schemes irrespective of the number of harmonics being eliminated. This reveals that the total harmonic distortion in any symmetrical PWM schemes remains same. Thus in the scheme in which lower-order harmonics are lower will have higher magnitudes for higher-order harmonics. However, the filtering of higher-order harmonics is easier, whereas the filtering of lower-order harmonics will require expensive filter. In this context, the scheme which results into low lower-order harmonics should be preferred.

2) For elimination of same number of harmonics, the scheme with odd number of pulses shifts the harmonic spectrum into higher order. Hence as explained above, choice of odd pulse modulation schemes would be more effective in harmonic control.

3) With three number of pulses/half-cycle third and all triplen harmonics can be eliminated. Thus, this scheme will be more economical for power control of heating appliances operating on single-phase or three-phase four-wire systems. However, with two pulses/half-cycle all the harmonics will be present in the line current.

6.2.5 Power Circuit for Realisation of Multi-Pulse per Half-Cycle

Figure 6.4(a) shows the proposed ac chopper circuit which operates on current commutation. S_1 is a main thyristor and S_2 is an auxiliary thyristor to commutate S_1. The auxiliary source enables the charging of commutating capacitor C independent of load. Capacitor C_1 smoothens the auxiliary voltage. Resistance Rh has ohmic value much higher that the load resistance. As the commutation circuit, unlike the one described in the previous chapter [18], is independent of the number of forced commutation per half cycle, this circuit can be employed to realise any number of chops (pulses) per half cycle in the load voltage.

On triggering S_1, while line 'a' is positive, the load current flows through line 'a' - D_1-S_1-D_3-R- line 'b'. When S_2 is triggered to commutate S_1, the commutating capacitor C reverses its polarity via the resonant loop C-S_2- commutating inductor L-C, causing the resonance current i_c. After half

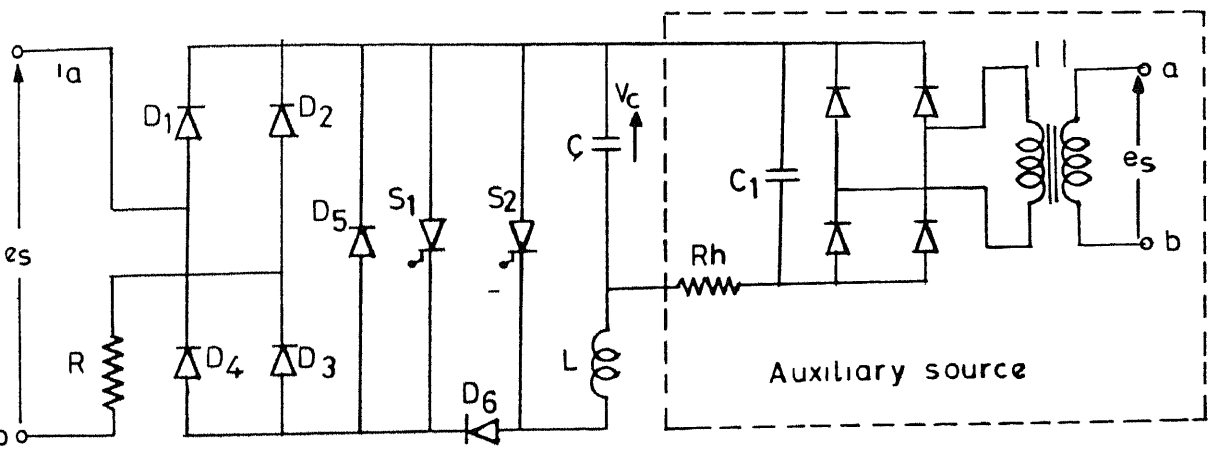


FIG.6·4(a)Power circuit for A.C. Controller

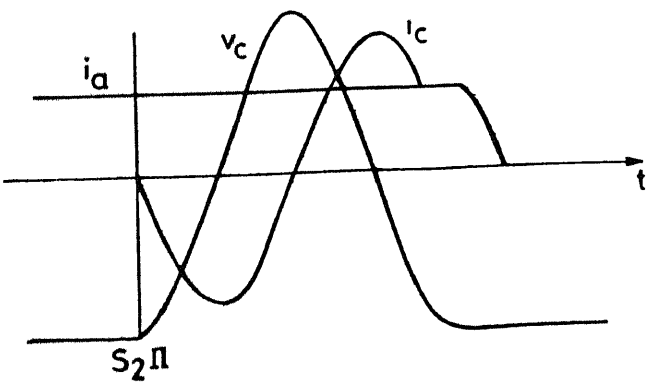


Fig. 6·4(b) Typical waveforms during commutation period

resonance time ($\pi\sqrt{LC}$), i_c goes through zero which turns off S_2. During the next half cycle of resonance, i_c flows through C-L-D_6-S_1-C until i_c becames equal to the load current i_a at which S_1 gets turned off. Afterward, i_c flows through D_5 and S_1 is reverse-biased by the forward voltage drop of D_5. The circuit turn-off time for which $i_c - i_a > 0$ can be adjusted by selecting proper values of L and C. D_5 turns off at the time when i_c decreases and becomes equal to i_a. Thereafter, the load current i_a, which is also a capacitor current i_c, flows through line 'a'-D_1-C-L-D_6- line 'b' and ultimately reduces to zero. The commutation period - the time interval between application of trigger pulse to S_2 and the load current zero - is relatively negligible compared to the pulse-width 2d. At the end of commutation C gets charged to voltage V_c. Capacitor current i_c and capacitor voltage v_c during the commutation interval are shown in Fig. 6.4(b). Each time when S_1 and S_2 are switched on, the circuit follows the operation as described.

This chopper has the following advantages over the one described in Chapter 5.

(i) The present circuit requires fixed number of commutating elements irrespective of number of harmonics being eliminated, and hence more economical while eliminating more than one harmonic.

(ii) As the present circuit works on current commutation, the line current consists of sinusoidal current segments. Whereas in the other one, which is operating on voltage commutation, the line current consists of sinusoidal segments with superimposed spikes due to voltage spikes during the commutation.

6.2.6 Control Circuit for Realisation of Five Pulses per Half Cycle

Fig. 6.5 shows the block diagram of the control scheme. The detail of the various signal waveforms is given in Fig. 6.6. In the present scheme and the scheme for ac-dc converter described in Chapter 4, the method of generating the signal E is the same. Hence the circuit detail given in Fig. 4.8(a) holds good for the present case also. Waveform M in Fig. 6.6 is derived by triggering the monostable at the negative going of E (Fig. 6.5). E and M, after amplifying and isolation, appear at the gates of the thyristors S_1 and S_2 respectively.

6.2.7 Experimental Verification

AC chopper circuit (Fig. 6.4(a)) operating on 230V,50Hz and the control circuits for power control in resistive load by 3rd, 3rd and 5th and 3rd,5th and 7th harmonics elimination schemes were constructed. Load power was varied from zero to the rated value by varying the control voltage. The corresponding rms values of line voltage and current were measured by moving iron type voltmeter and ammeter,and the load power was

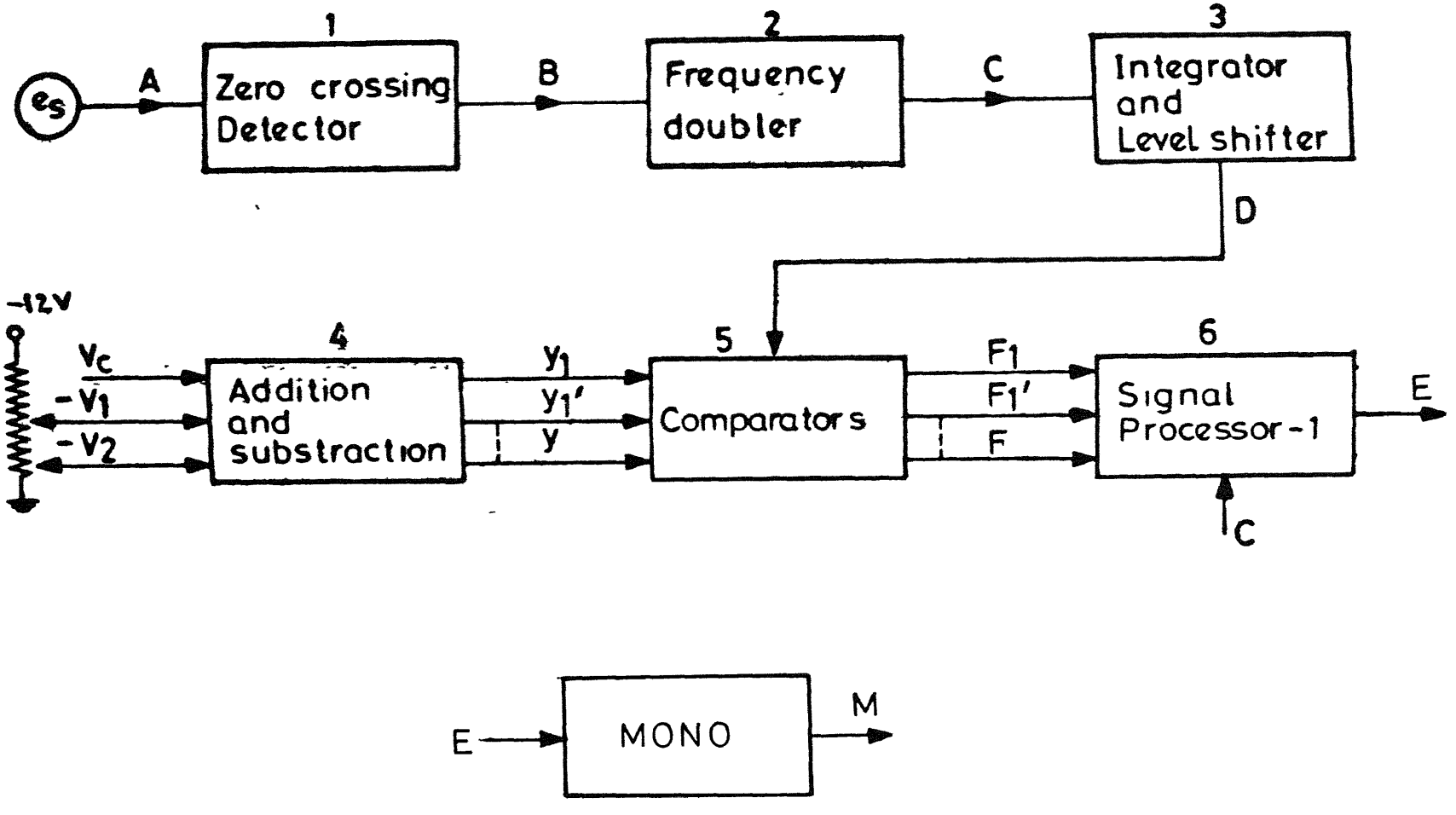


Fig.6·5 Block diagram of the control scheme

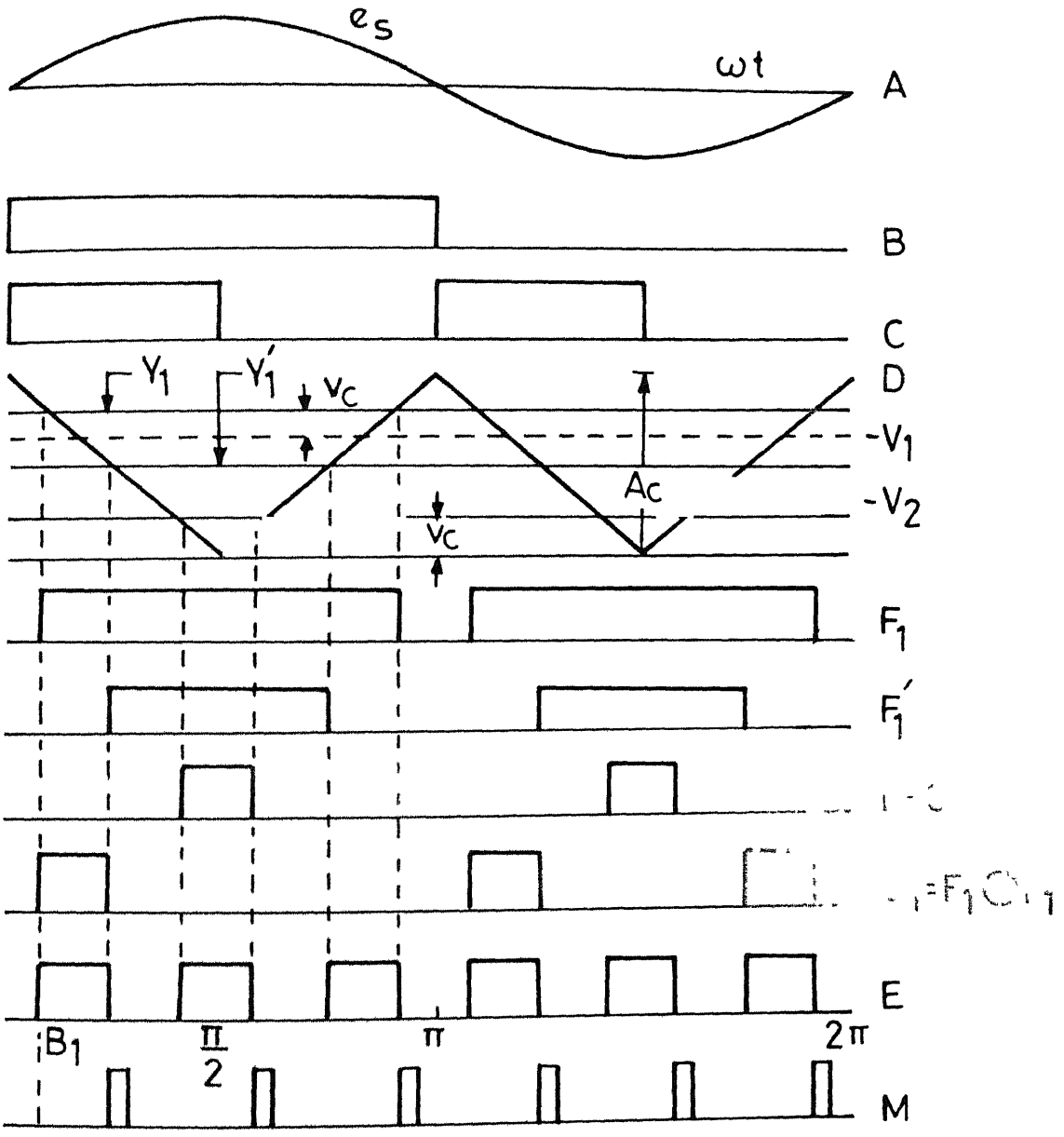


Fig.6·6 Timing diagram of fig.6·5

measured by dynamometer type wattmeter. From the measured quantities the power factor and peak fundamental line current were computed as

$$p.f. = \frac{W}{E_{rms} \cdot I_{rms}}$$

and

$$I_1 = \frac{\sqrt{2}\, W}{E_{rms} \cos\phi}$$

$$= \frac{\sqrt{2}\, W}{E_{rms}} \text{ (as for resistive load } \cos\phi = 1)$$

The different measured values and the calculated values of power factor and the peak fundamental current are tabulated in Table 6.1.

Fig. 6.2 shows that the experimental and theoretical results agree satisfactorily. The apparent discrepancy may be attributed to the measurement errors. However, due to non-availability of spectrum analyzer, harmonics measurements could not be performed. Fig. 6.7(a) shows the control circuit waveforms and Figs. 6.7(b) and (c) show the line-voltage and line-current waveforms for 3rd and 3rd, 5th and 7th harmonic elimination schemes.

6.3 METHOD OF SELECTIVE HARMONIC REDUCTION

In Section 6.2.3 a third harmonic elimination method employing three pulses per half cycle has been described.

Table 6.1

Experimental Values

I_m = 13.4A (= 1 p.u.)

Load resistance, R = 22.5 Ohms

Harmonic elimination	Measured values of input quantities			calculated values	
	E_{rms}	I_{rms}	W	p.f.	I_1/I_m
3rd	232	5.4	750	0.59	0.327
	232	7.1	1200	0.728	0.526
	230	8.35	1700	0.885	0.752
	230	8.8	1900	0.938	0.84
3rd,5th	225	4.6	525	0.507	0.25
	225	6.0	916	0.65	0.43
	222	7.4	1325	0.806	0.634
	220	8.7	1850	0.966	0.80
3rd,5th,7th	232	4.3	483	0.451	0.22
	230	5.85	900	0.668	0.397
	230	7.1	1307	0.76	0.60
	230	9.0	1950	0.942	0.846

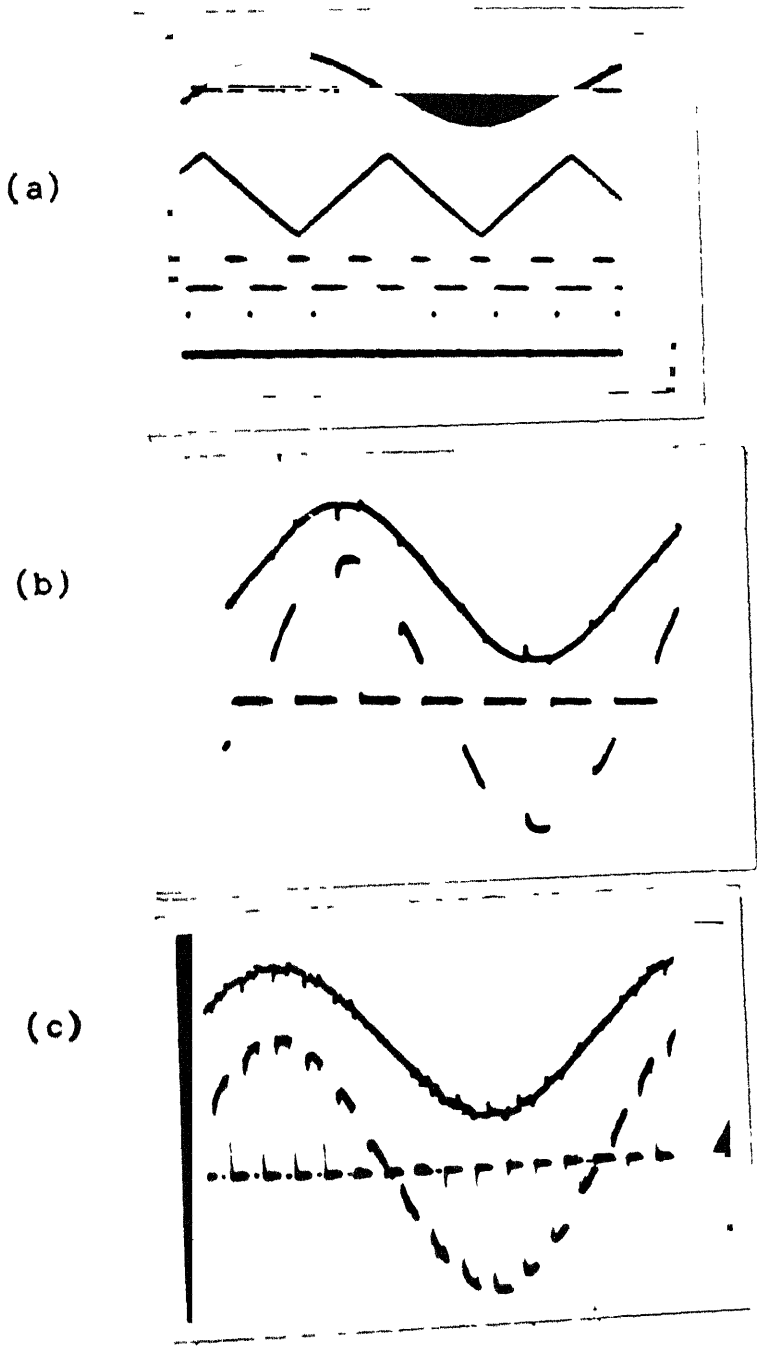


Fig. 6.7 Oscillograms for selective harmonic reduction in ac controller with R load

(a) Control circuit waveforms A,D,E and M for 3rd harmonic elimination
(b) Third harmonic elimination : Top : Line voltage ; Bottom : Line current
(c) Third, fifth and seventh harmonics elimination Top : Line voltage ; Bottom : Line current

However, that method is applicable only to eliminate triplen harmonics. To minimize any one unwanted line current harmonic, the method proposed here assumes three pulses per half cycle of the line voltage which are located symmetrically about $\pi/2$ axis at B_1,B_2 and B_3 as shown in Fig. 6.8(a), where

$$B_2 = \pi/2$$

$$B_3 = \pi - B_1$$

$$\alpha_i = B_1 - d \quad \text{for} \quad i = 1 \text{ to } 3$$

and $$\beta_i = B_1 + d$$

Power control is affected by varying the pulse width symmetrically around the pulse position. To minimize a selected harmonic the pulse position is decided on the following basis.

Initially, assume line current to be flat-topped of amplitude I'_m as shown in Fig. 6.8(b). Fourier analysis of the waveform of Fig. 6.8(b) gives the following results :

$$a_n = 0$$

$$b_n = \frac{8I'_m}{n\pi} \sin nd \left(\sin nB_1 + \frac{1}{2} \sin \frac{n\pi}{2}\right) \qquad (6.14)$$

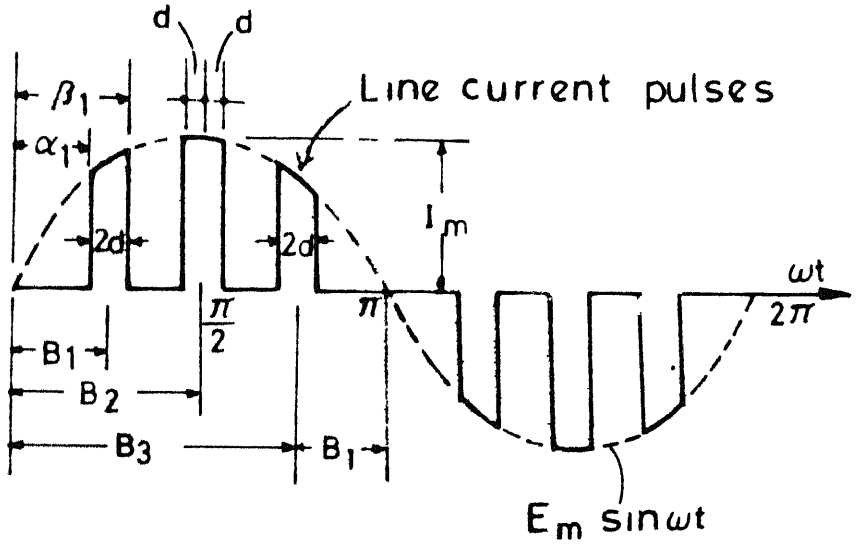
where n = 3,5, ...

From eqn. (6.14), for nth harmonic to be zero

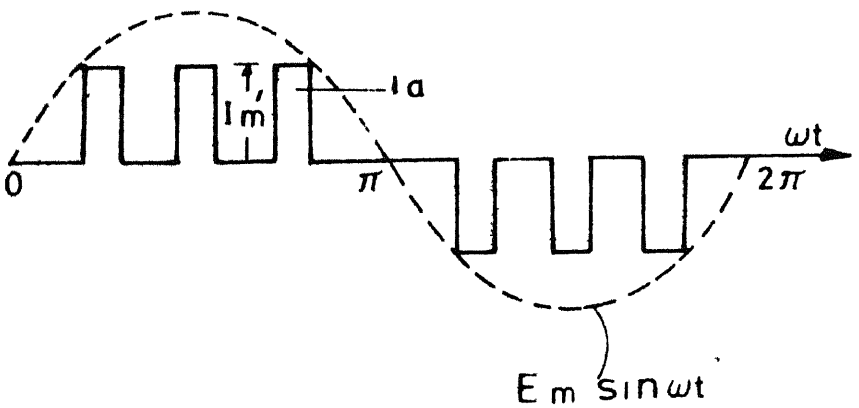
$$\sin nB_1 + \frac{1}{2} \sin n\pi/2 = 0 \qquad (6.15)$$

with the constraint

$$B_1 < \pi/2 \ .$$



(a)



(b)

Fig. 6·8 Third harmonic reduction

(a) Actual line current waveform

(b) Flat-topped line current waveform

For a selected harmonic of order n, eqn. (6.15) may have more than one solution for B_1. In that case, the one which results into better performance - lower dominant harmonic, lower minimized harmonic and higher control range (output voltage) - should be chosen. For example, for n = 5 two solutions are $B_1 = 42^\circ$ and 66°. Out of these, $B_1 = 42^\circ$ gives better performance as shown in Table 6.2.

In the alternative method [30], which employs two pulses per half cycle, located at B_1 and $\pi - B_1$, the harmonic coefficient with flat-topped current are given by

$$a_n = 0$$

and

$$b_n = \frac{8I'_m}{\pi n} \sin nd \sin nB_1$$

Hence, for elimination of nth harmonic

$$B_1 = \frac{\pi N}{n} \tag{6.16}$$

where N is an integer number and $B_1 < \pi/2$.

However, in Ref [30] B_1 is chosen as $B_1 = \pi/n$. Instead of such unique choice, a better choice may be made from eqn. (6.16). For example, for n = 5 in eqn. (6.16) $B_1 = 36^\circ$ and 72°. However, the latter one gives better performance (Table 6.2).

Table 6.2 Maximum Value of Harmonics as a Percentage of I_m

Harmonic order	Percentage maximum value of harmonics = (b_n/I_m)			
	3rd Harmonic reduction		5th Harmonic reduction	
	Proposed method P = 3	Alternative method P = 2	Proposed method P = 3	Alternative method P = 2
3	13.8	13.8	3.57(39.6)	29.6(40.5)
5	13.8	35.5	5 (3.12)	3.12(25.23)
7	20	28.5	38.6 (13.8)	19 (21.5)
9	35	5	22.5 (7.6)	22.5 (10)
Maximum output-voltage	$0.686V_m$	$0.686V_m$	$0.703V_m$ ($0.593V_m$)	$0.593V_m$ ($0.554V_m$)
Pulse position B_1	50°	60°	$42^\circ(66^\circ)$	$72^\circ(36^\circ)$

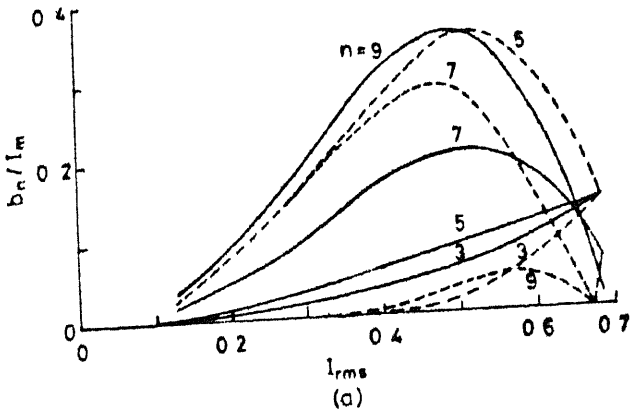
In the above, the pulse position has been fixed considering flat-topped current pulses. However, actual line current as shown in Fig. 6.8(a) consists of sinusoidal current segments. Therefore, the pulse placements as above will not eliminate the selected harmonic completely but will reduce it to a sufficiently small value as shown later.

6.3.1 Comparison of the Proposed and Alternative Methods

Reduction of 3rd and 5th harmonics are studied by both the methods for their comparison. Using eqns. (6.4) to (6.10) which hold good here also, power factor and the dominant harmonics are computed for different values of d. As usual for PWM schemes, Fig. 6.2 shows the p.f. and fundamental current variation for both the methods. Figs. 6.9(a) and (b) show the variation of the normalized amplitudes of dominant harmonics with the normalised rms load current in both the methods in reducing 3rd harmonic and 5th harmonic, respectively.

The salient features of both the methods are given in Table 6.2. The following important points may be noted from the figures and the table :

i) The variation of p.f. and the fundamental line current are the same in both the methods and independent of the harmonic being reduced. This implies that the total harmonic distortion also remains the same in both the methods.



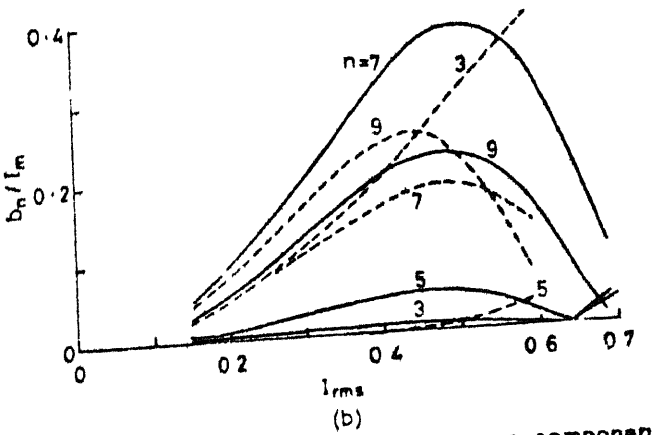


Fig 6·9 Variation of line current harmonic components
—— Proposed scheme
----- Alternative scheme
(a) 3rd harmonic reduction
(b) 5th harmonic reduction

ii) In 3rd harmonic reduction, 5th and 7th harmonic contents in the proposed method are much lower, however, 9th harmonic is higher which can be easily filtered out. The maximum output voltage is the same in both the methods.

iii) In the case of 5th harmonic reduction, the proposed scheme has higher output voltage and much lower 3rd harmonic content.

From the above it can be seen that proposed method provides better control range and has less lower order harmonic, which will reduce the filter cost.

6.4 CONCLUSIONS

A general method of elimination of any number of line current harmonics and a method of reduction of any one line current harmonic, employing odd number of pulses per half cycle, have been presented. In both the methods, the pulses are of equal widths and they are located at fixed positions. Power control is obtained by varying the pulse widths symmetrically around the pulse positions. The comparison of the present schemes with the alternative schemes employing even pulses/ half cycle shows that the former ones are more effective in harmonic control because in the case of harmonic elimination the

dominant harmonics are pushed more into higher order spectra, and in the case of harmonic reduction the dominant harmonics are reduced more. A new power circuit and control circuit for the practical realisation of the general method has been described. Experimental results show the feasibility of implementing the schemes.

CHAPTER 7

POWER FACTOR IMPROVEMENT BY STATIC VAR COMPENSATORS

7.1 INTRODUCTION

In the power system, the lagging reactive power is mainly attributed to induction motor load which constitutes nearly 40% of the total load on the power system. The induction furnaces and the arc furnaces also consume large amount of reactive power. The thyristor controlled rectifiers and ac voltage controllers, which are now widely used, also contribute large amount of lagging reactive power. This causes the system to operate at low power factor. Until recently, the mechanically switched capacitor/reactor banks and synchronous condensers have been used for compensating the load reactive power. However, they have limitations of slow response, large maintenance and generation of switching transients in the former ones.

With the increase in the size and complexity of power system networks, fast reactive compensation has become necessary in order to maintain the stability of the system and efficient transfer of power. This has yielded the development of static reactive power (VAR) compensators (abbreviated as SVCs) which employ thyristor switch modules to control capacitor/reactor elements. Thyristor switches allow perfectly synchronised transient-free switching of reactive elements, which enables

SVC to adjust the compensating current in each half-cycle of the supply cycle. Due to their fast response and flexible control, SVCs are finding increasing acceptance in i) the industrial sectors for load balancing, power factor correction and suppression of voltage fluctuations due to rapidly changing reactive power by arc furnace and rolling mills [35-37], and, ii) the utility systems for regulating the transmission line voltage, limiting overvoltages due to line switching or loss of load and increasing the system damping factor for improvement of transient stability[37-41].

Different circuit configurations of SVCs, and, their operation, control and suitability to different applications have been described in the literature [32-35]. Although, the control circuits form an integral part of the SVC systems, whose reliability and accuracy of control immensely depend upon the control scheme used, their details have not been explored. In the thyristor-switched capacitor thyristor-controlled reactor (TSC-TCR) and TSC types compensators, the control strategy of applying the gate pulses to the thyristors of TSC at the peaks of the supply voltage [32] is inadequate for transient free switching of capacitors. This is, because, the voltage across the capacitor bank prior to switching-in can be of any value between peak-to-peak of supply voltage, and, that may cause large inrush current in the lines. To limit the inrush current, it requires an appropriate size of inductor in series with each

bank. For the control of compensators involving TCR, the normal method followed for adjustment of TCR current is to solve the nonlinear function relating TCR current and firing angle α in real time [35]. However, for the compensators used in industries this approach seems to be little cumbersome and some simple approach is required.

This chapter presents the operation and control of TSC and FC-TCR types compensators for power factor correction. A control scheme for TSC compensator has been presented which initiates the trigger pulses at the zero of the voltage across the thyristor switch module. This eliminates the inrush current and thus the series inductor in the capacitor bank. Also, a control scheme, based on feed-forward control, is presented for FC-TCR compensator in which the real time computation has been avoided using look-up table algorithm. This simplifies the implementation of control and improves the system reliability. Both the schemes have been realised and the experimental results for steady-state and transient operation are presented.

The current in TCR is nonsinusoidal, which gives rise to harmonics in the supply current. Unless the harmonics are filtered out or controlled, they will adversely affect the power system. In this chapter, a method is proposed to reduce the harmonics due to TCR current. Unlike the conventional method, in the proposed method the TCR is supplied from a

transformer with a tapped secondary. The taps are operated sequentially to control the reactor current. Two alternative schemes are given for the sequence control of the transformer taps, and the line current harmonics in these schemes have been compared with that of conventional method. The feasibility of both the schemes proposed has been verified experimentally.

7.2 REACTIVE POWER COMPENSATION BY THYRISTOR-SWITCHED CAPACITORS

Normal practice followed in industries is to install fixed capacitors for compensation of inductive loads. This results in either under or over compensation which is an undesirable feature. Reactive power varying at slow rate may be compensated by installing series of capacitor banks and switching one or more banks in or out mechanically depending upon reactive power demand. However, this introduces switching transients and it is inadequate to provide dynamic compensation for the loads like rolling mills, arc furnaces etc.

Thyristor switched capacitors, which replace conventional mechanical switches by thyristor switch modules, provide efficient means for dynamic compensation of lagging reactive power. Thyristors enable transient free switching of capacitor bank. With intelligent control TSC may be operated for power

factor correction or damping of power system oscillations. In the following the thyristors switching of capacitors is described and a control scheme for power factor correction is presented.

7.2.1 Operating Sequence of Capacitor Banks

Power circuit of the basic TSC compensator is shown in Fig. 7.1. It comprises n capacitor banks each of value C and a pair of antiparallel thyristors in series with each bank. C and n are chosen on the following basis :

Let I_{ar} = amplitude of the reactive load current

and I_{lag} = maximum value of I_{ar}

For compensation of maximum reactive current, the compensator current, when all the banks are switched-on should be equal to I_{lag}, i.e.,

$$I_{lag} = \omega n C E_m \tag{7.1}$$

As per the load demand, the compensator current is controlled by operating the capacitor banks in sequence. Operating sequence of the capacitor banks is given by eqn. (7.2).

$$I_{ari} = \frac{(2i-1)\, I_{lag}}{2n} \tag{7.2}$$

where i = 1 to n (bank number).

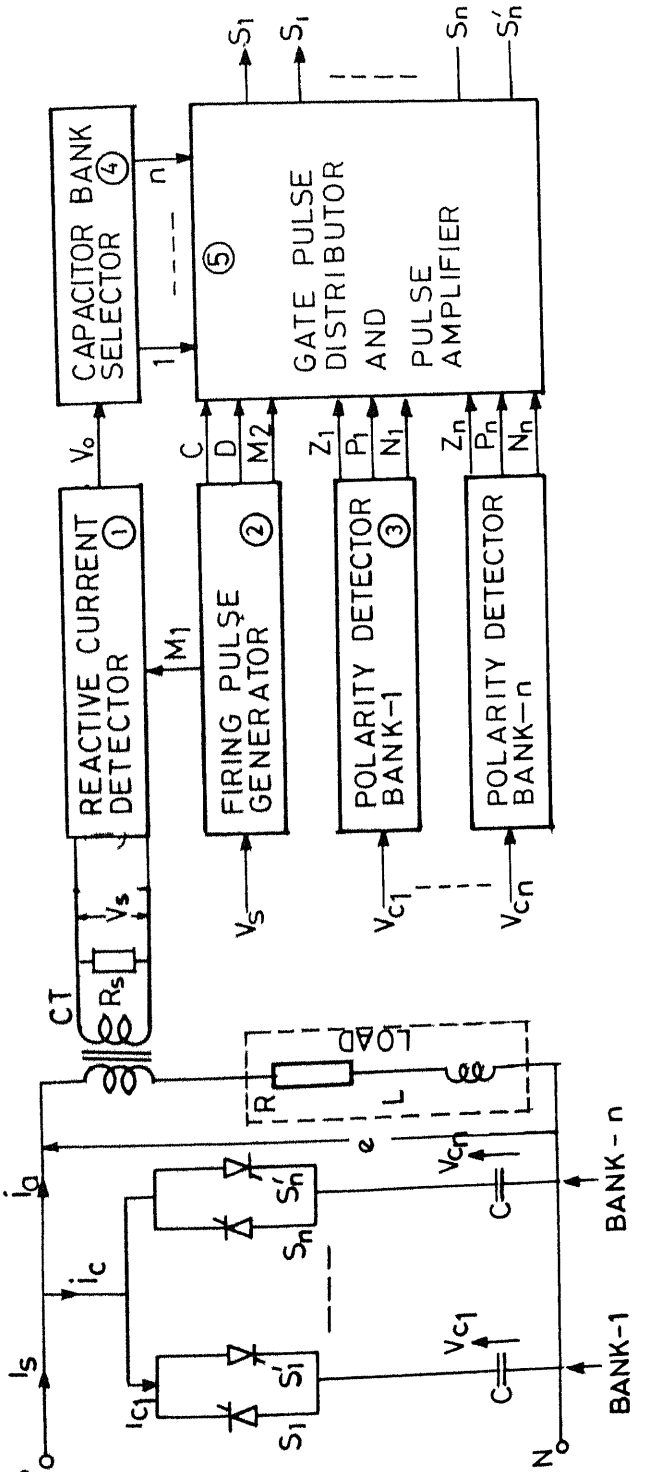


Fig.7.1 Basic TSC compensator and the block diagram of the control scheme

In eqn. (7.2), ith bank will be switched in when the reactive load current I_{ar} exceeds the set level I_{ari}, and it will be switched out when I_{ar} falls below the set level. Resulting compensator current with reactive load current is shown in Fig. 7.2, where, points A_1 to A_n correspond to the switching levels of banks 1 to n. As the compensating current varies in steps,it results in under/over compensation. The maximum error in the compensation occurs at the switching points and is given by

$$\Delta I_{lag} = \pm \frac{I_{lag}}{2n} \qquad (7.3)$$

Compensation error could be kept to a reasonably small value by using a large number of small sized capacitor banks. However, the system cost and power losses due to thyristor switching increase. Therefore, appropriate number of capacitor banks are chosen on the basis of economy and the permissible compensation error.

7.2.2 Transient-free Thyristor Switching of Capacitors

Switching-on transients in TSC can be avoided by triggering the thyristors at the instant when the supply voltage corresponds in magnitude and polarity to the capacitor voltage. Switching-off of the thyristors occurs at the next current zero after the removal of the gate pulses. Voltage on the capacitor at the instant of switching-off will be either equal to positive

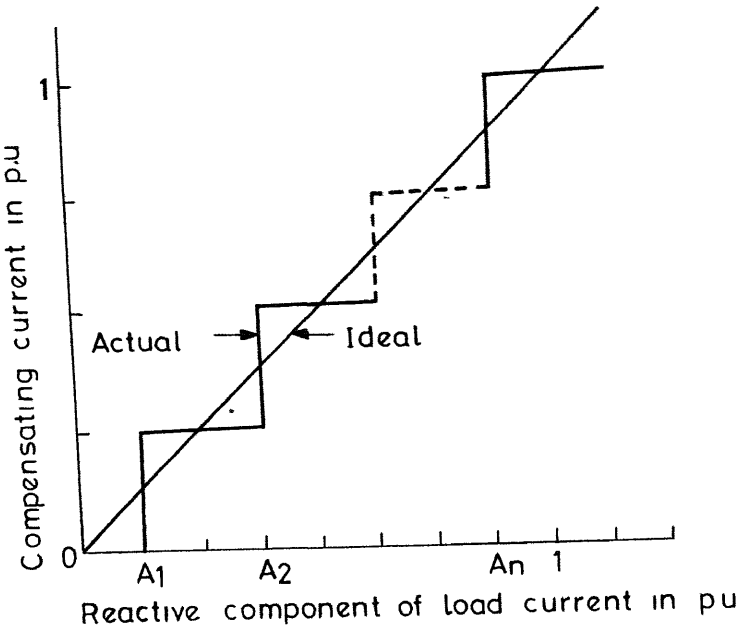


Fig 7-2 Operating sequence of the capacitor banks

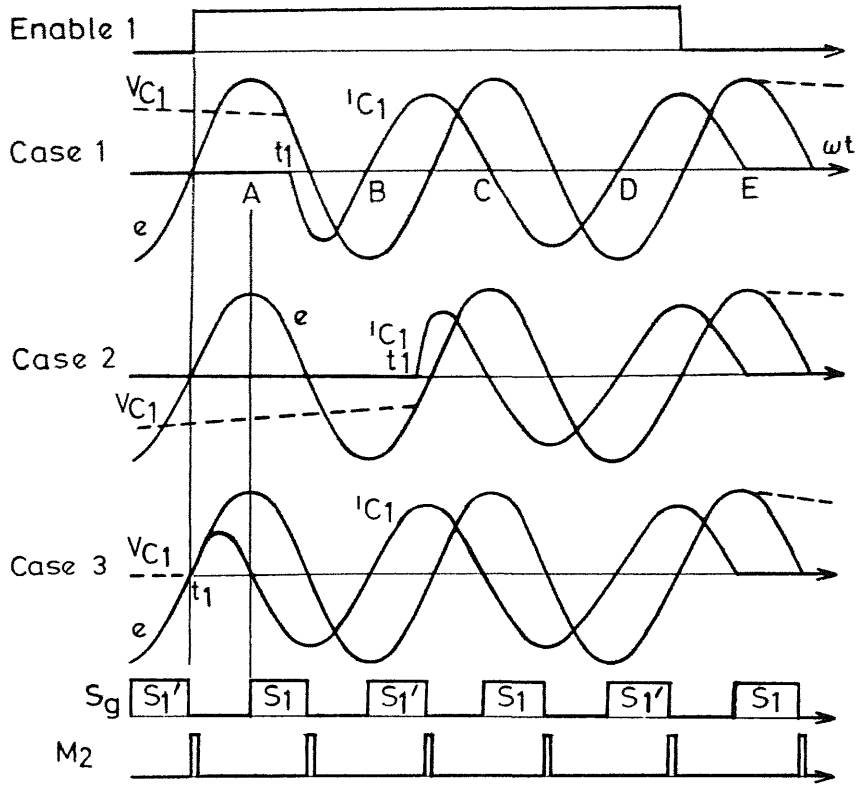


Fig 73 Switching in of capacitor bank at different initial voltages on the capacitor

or negative peak value of the supply voltage. In course of time, capacitor voltage decays to zero due to capacitor leakage or discharging resistor.

Initial voltage on the capacitor, prior to switching-on, depends upon its previous state in the network, and, it may be at any value between positive and negative peak values of the supply voltage. Fig. 7.3 illustrate the principle of transient free switching-on of capacitor bank-1 under different initial capacitor voltages. In the figure, e ,v_{c1} and i_{c1} represent supply voltage and voltage and current in bank-1, respectively. It necessarily needs a pulse train M_2 of narrow pulse width occurring at zero crossings of the supply voltage and, a pulse train S_g consisting pulses S_1 and S_1' of 90^o width which occur at positive and negative peak values of supply voltage respectively. Control signal 'Enable-1' is governed by the reactive current demand. It is at logical high level when $I_{ar} > I_{ar1}$. On receipt of Enable-1 high, as dictated by the initial capacitor voltage for transient free switching-on, the firing pulses to the thyristors should appear in the following order. For positive capacitor voltage, pulse S_1 appears at the gate of thyristor S_1. For negative capacitor voltage, pulse S_1' appears at thyristor S_1'. And, for zero voltage on the capacitor, pulse M_2 appears simultaneously at the gates of S_1 and S_1'. Switching operation under these three cases is described below.

Case-1 : Initial capacitor voltage positive

Thyristor S_1 receives pulse S_1 at instant A. Since S_1 is reverse biased between the interval A and t_1, it turns on only at t_1 where capacitor voltage is equal to supply voltage. During the period thyristor conducts, capacitor voltage follows the supply voltage. At instant B, i.e., at the negative peak of the supply voltage, S_1 turns off as the current through it goes to zero. At this instant capacitor voltage is negative and equal to the supply voltage. Hence, the application of pulse S_1' to thyristor S_1' keeps capacitor connected to the supply through S_1'. So long 'Enable-1' is high, application of the trigger pulses at the peaks of the supply voltage keeps capacitor on. In this case, delay time t_1 - time between the occurrence of Enable-1 and switching-on instant - is less than half-cycle.

Case-2 : Initial capacitor voltage negative

Thyristor S_1' receives trigger pulse S_1' at instant B. Between the instants B and t_1, S_1' is reverse biased. At t_1, v_{c1} and e are equal and S_1' becomes forward biased. Therefore, at t_1, S_1' turns on without any inrush current. For this case switching delay t_1 is less than a cycle.

Case-3 : Initial capacitor voltage zero

In this case both the thyristors receive pulse M_2 simultaneously. As thyristor S_1' is forward biased it conducts at

zero of the supply wave, reverse biasing S_1. Capacitor voltage follows the supply wave. At instant A, current through S_1' goes to zero value which turns off S_1'. Since at point A capacitor voltage is positive and equal to the supply voltage, pulse S_1 at the instant A turns on S_1 without current inrush and keeps capacitor on. In this case, the switching-on delay time t_1 is zero.

In all the above cases, when Enable-1 becomes zero, the trigger pulses to the thyristor-switch module are blocked and the conducting thyristor comes to blocking state at the next current zero, i.e., at the peak of the supply voltage. Thus, the capacitor is switched off with a maximum delay of half-cycle.

A control scheme based on the above principles is described below.

7.2.3 Proposed Control Scheme

Since the conducting thyristors in the TSC compensator cannot be turned off within their conduction period, reactive current can be adjusted only at the discrete instants of time, which correspond to the instants of the peak of the supply voltage. Between any two such consecutive time instants, by sensing the load current, the reactive current of the load may be computed for the control of compensator current. Based on this, a direct computational scheme, called feedforward control is devised for TSC compensators which is inherently stable, fast

and quite adequate for power factor correction. In the proposed scheme, the load current is assumed to be in the steady-state between any two consecutive instants of time at which compensator current changes. With this assumption, reactive component of the load current may be computed in a simpler manner as follows.

The fundamental load current between the said instants with reference to input voltage $e = E_m \sin \omega t$, may be written as

$$\begin{aligned} i_a &= I_a \sin(\omega t - \phi) \\ &= (I_a \cos\phi) \sin\omega t + (-I_a \sin\phi) \cos\omega t \\ &= I_{a\omega} \sin\omega t + I_{ar} \cos\omega t \end{aligned} \qquad (7.4)$$

where $I_{a\omega}$ = amplitude of the active current

I_{ar} = amplitude of the reactive current

and ϕ = load power factor angle.

From eqn. (7.4), it is evident that the magnitude of the reactive current in each half-cycle may be derived by sampling the load current at the zero crossing points of the supply voltage.

Fig. 7.1 shows the block diagram of the proposed scheme. Figs. 7.5(a) and (b) show the timing diagrams of the control scheme.

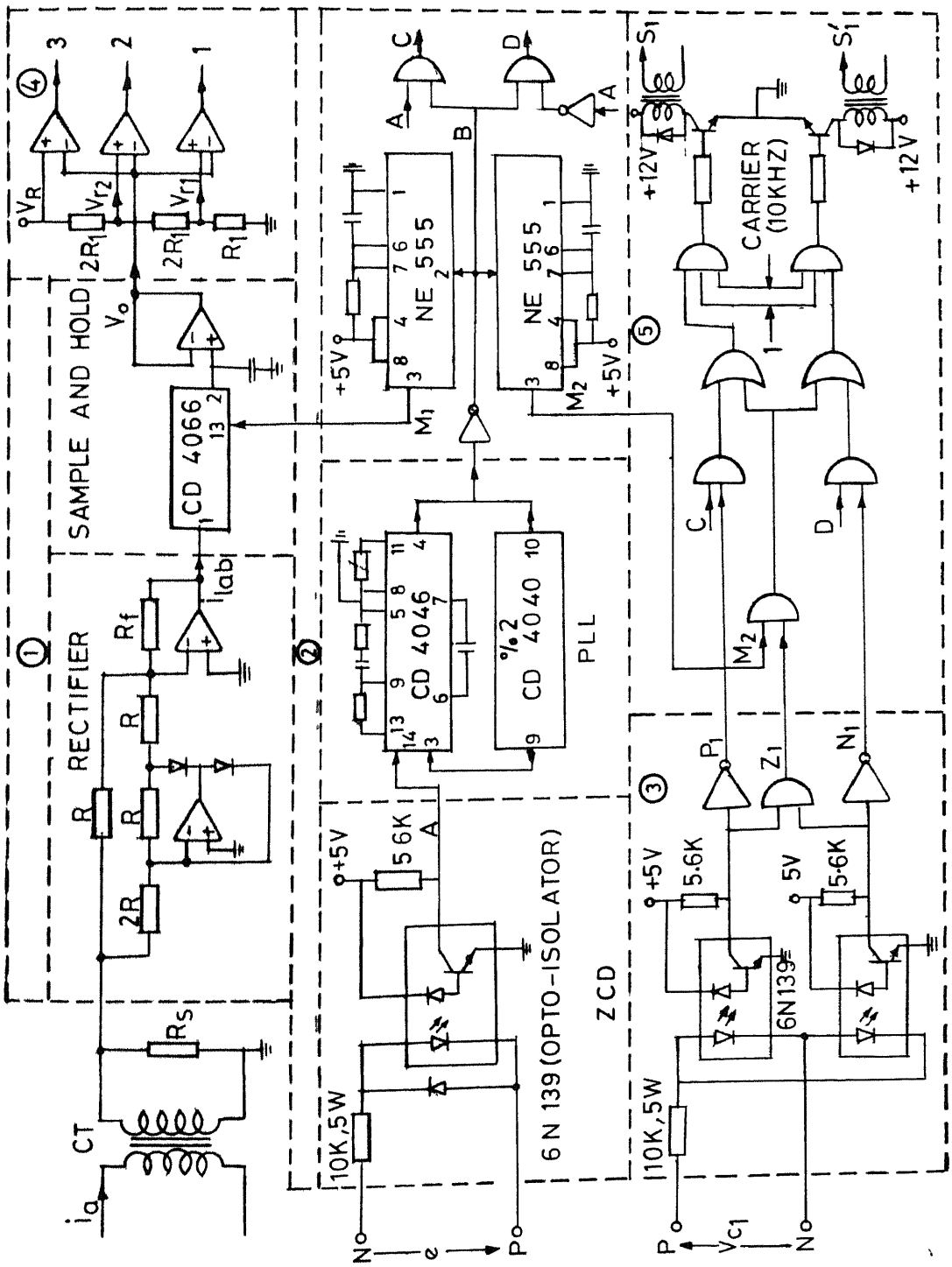
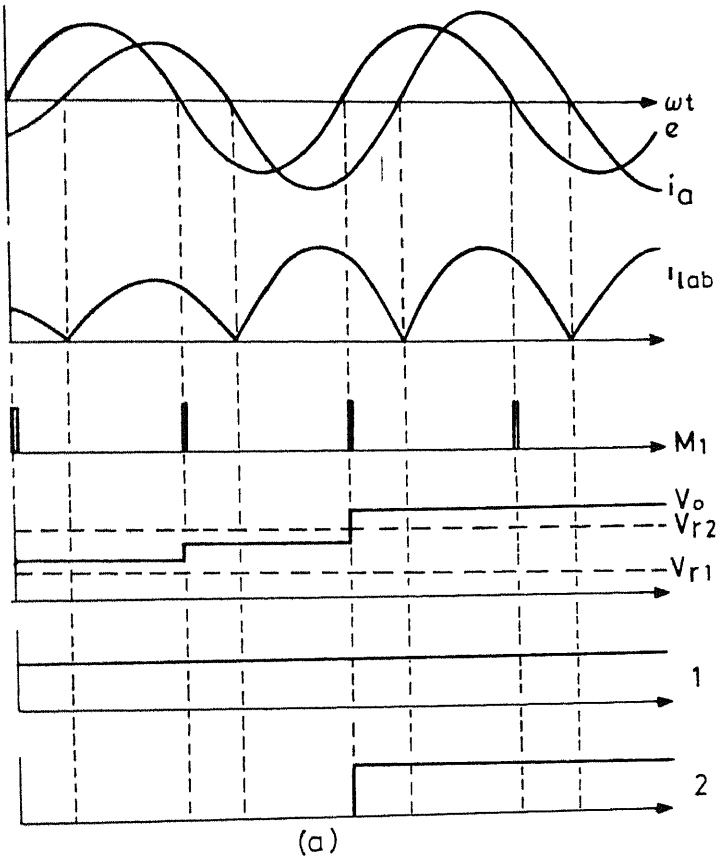
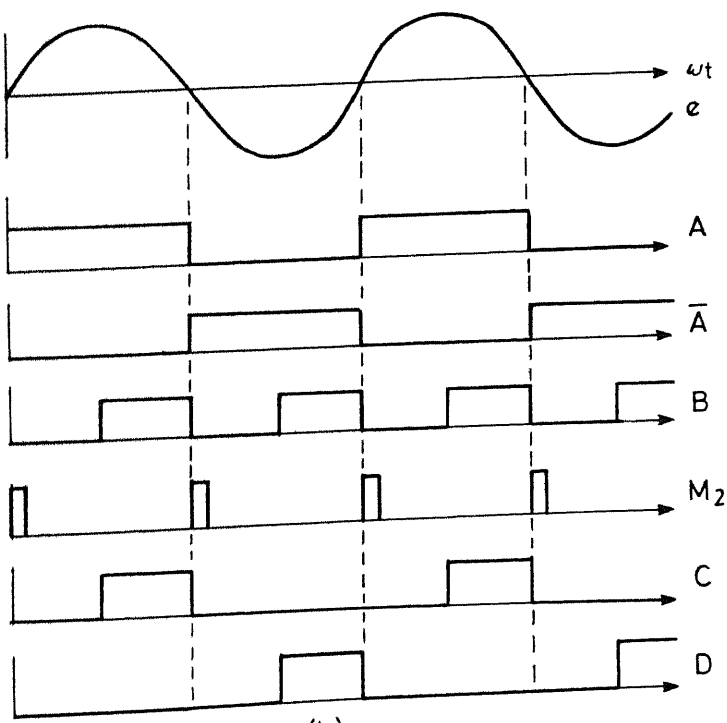


Fig 74 Circuit diagram of the control scheme



(a)



(b)

Fig 75 Timing diagrams (a) Reactive current detector and capactor bank selector (b) Firing pulse generator

The load current sensed through current transformer (CT) is applied to the reactive current detector, which provides dc output V_o proportional to the peak reactive load current. V_o is fed to the capacitor bank selector (CBS) comprising of n number of compensators which are set for different levels in accordance with eqn. (7.2). Outputs of CBS determine the number of banks to be switched in or out by enabling or disabling the gate pulses to the thyristors of the respective banks. Polarity detector of each bank determines the state of the voltage of the capacitor bank. For example, for ith bank the variables (P_i, N_i, Z_i) will have logical values (1,0,0), (0,1,0), (0,0,1) for capacitor voltage positive, negative and zero respectively. The pulses C,D and M_2 of the firing pulse generator correspond to the pulses S_1, S_1' and M_2 respectively in Fig. 7.3. For positive, negative or zero voltage of the capacitor banks to be switched on (as determined by CBS), the pulse distributor will transmit either C,D or M_2 respectively to the gates of the corresponding thyristors.

In this scheme, the reactive current is measured in the half-cycle preceding the one in which the correction is applied. From Fig. 7.3 it can be seen that the transient response time is less than one cycle of the supply.

7.2.4 Implementation of the Control Scheme

Fig. 7.4 shows the detailed circuit diagram of the proposed scheme which has been implemented using digital circuits.

Reactive current detector :

Load current is sensed by a CT and rectified by a precision rectifier formed using operational amplifiers. A sample and hold circuit, consisting of an analog gate and op-amp, samples the rectified quantity at zero crossings of the supply voltage to produce V_o proportional to the magnitude of the reactive current. The phase error, introduced by the CT and the associated filters, may be compensated by providing same amount of phase-shift to the sampling pulses M_1.

Capacitor bank selector :

CBS comprises op-amp comparators equal to the number of capacitor banks. Their one input receives V_o and the other input, as per the eqn. (7.2), is set to a level given by

$$V_{ri} = V_R\left(\frac{2i-1}{2n}\right)$$

where $V_R = V_o$ at the maximum reactive current I_{lag}. When V_o exceeds V_{ri}, firing pulses are enabled to switch-in ith bank. As the value of V_o changes only at the sampling instants, the outputs of CBS change their logical states only at the zero crossings of the supply voltage.

Firing Pulse generator :

Supply voltage e is digitised to generate square wave A using a opto-isolator which provides a perfect isolation between the power circuit and the control circuit. Using PLL circuit [42], frequency of A is multiplied by 2 to generate B. C is derived by ANDing A and B, and D is derived by ANDing $\bar{A}$ and B. Due to PLL the positions of C and D with respect to the supply wave do not change with the drift in the supply frequency. Pulses M_1 and M_2 at the zero crossing instants of the supply voltage are produced by triggering two monostables at the negative going edge of B. Fig. 7.5(b) shows the timing diagram of the waveforms.

Polarity detector :

The scheme used for polarity detection, i.e., positive, negative or zero voltage on the capacitor bank, should work satisfactorily under switched-in as well as switched-off states of the capacitor and should provide electrical isolation between power and control circuits. Since the voltage on the off-bank is dc, the scheme employing transformer for isolation will be rather complex. Polarity can be detected in a simpler way by using opto-isolators. In Fig. 7.4, an antiparalleled opto-isolator pair in series with a resistance is connected across each bank to determine the polarity. For the switched-in capacitor, supply and capacitor voltages are the same. Hence P_i

follows A and N_i follows $\bar{A}$, whereas, Z_i remains at zero level.

Gate pulse detector and pulse amplifier :

Outputs of the CBS, firing pulse generator and polarity detector are wired logically using logic gates to generate the firing pulses in the required order, described in Section 7.2.2. The thyristor pulses of the ith bank follow the following logics :

$$S_1 = (C.P_i + M_2.Z_i).i$$

$$S_1' = (D.N_1 + M_2.Z_i).i$$

After modulating with 10 kHz carrier and amplifying, they are applied to thyristor gates.

7.2.5 Experimental Verification

Compensator performance was studied on an inductive load consisting of an inductor of 3 KVAR rating and a series connected variable resistance. Compensator considered had three capacitor banks each of 50 μF making the total capacity of 2.5 KVAR when operated from 230V, 50 Hz supply.

For steady state performance, input and load power factors were computed from the measured values of input voltage and power, input current and load current by varying the load resistance. Results are tabulated in Table 7.1 which reveals that the experimental performance is as expected.

Table 7.1 Experimental values for TSC Compensator

Line voltage = 230 V

Without compensation			With compensation		
Line/load current Amp	Power watts	p.f.	Line current Amp	Power watts	p.f.
4	875	0.951	4.0	875	0.951
5	1062	0.923	4.97	1072	0.938*
6	1225	0.888	5.44	1235	0.987*
7	1358	0.844	5.97	1370	0.998
8	1453	0.79	6.50	1465	0.979
9	1498	0.724	6.65	1510	0.988*
10	1477	0.642	6.53	1497	0.997
11	1360	0.537	6.25	1390	0.967*

*leading

To study the dynamic performance under continuously varying reactive power, reactive current detector was supplied from a low frequency oscillator instead of load currents. The oscillograms shown in Figs. 7.6(a) and 7.6(b) show the compensator operation to meet the continuously varying reactive current demands which are varying cyclically at 1.5 Hz and 4 Hz respectively. It can be seen in both the cases that, the sequential switching-in and out of all the three banks takes place without any transients and the compensator current is in resemblance with the reactive current demands. Fig. 7.7(a) shows the supply voltage and capacitor current waveforms and, Fig. 7.7(b) shows the capacitor bank voltage and thyristor gate pulse when the gate pulses are enabled with a square wave of 12.5 Hz.

Figs. 7.8 and 7.9 show the transient response of the compensator with the sudden change in the load parameters. In Fig. 7.8, the load is changed from highly resistive to highly inductive by cutting off the series resistance. During the transient period, the load current may have dc off-set which in turn depends upon the instant of switching. Therefore, the compensator performance during the load current transients depends upon the degree of off-set in the load current. Oscillograms in Fig. 7.9 show the performance when the load parameters are changed from a highly inductive value to a highly resistive value by inserting a resistance in the load circuit.

(a)

(b)

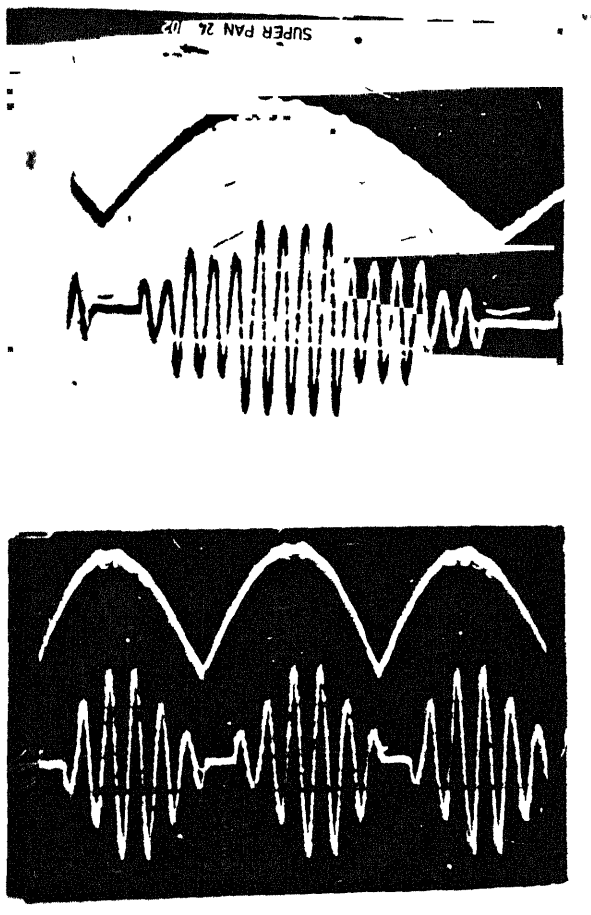


Fig. 7.6 Waveforms illustrating the operation of TSC compensator for continuously varying reactive current demands (dynamic response)
(a) Top : Reactive current demand with 1.5 Hz cyclic variations,
Bottom : Compensator current
(b) Top : Reactive current demand with 4 Hz cyclic variations,
Bottom : Compensator current

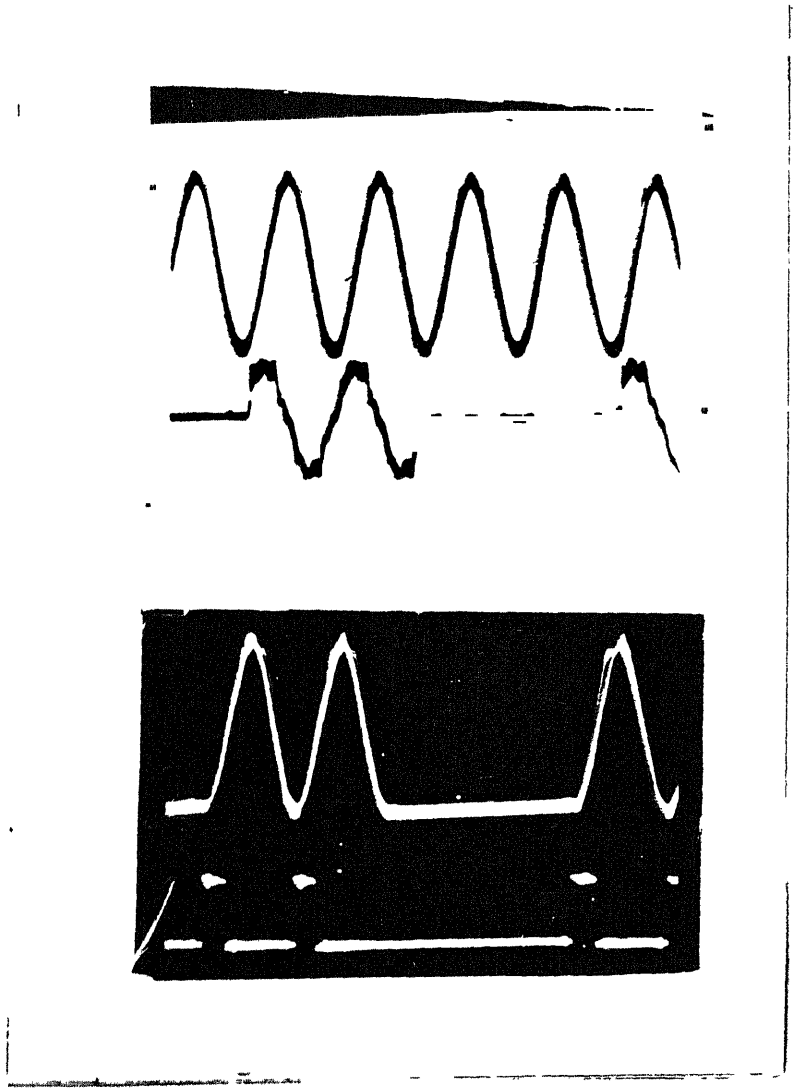


Fig. 7.7 Waveforms by 12.5 Hz cyclic switching of a capacitor bank
(a) Top : Supply voltage,
Bottom : Capacitor current
(b) Top : Capacitor voltage,
Bottom : Gate pulses to one of the thyristor

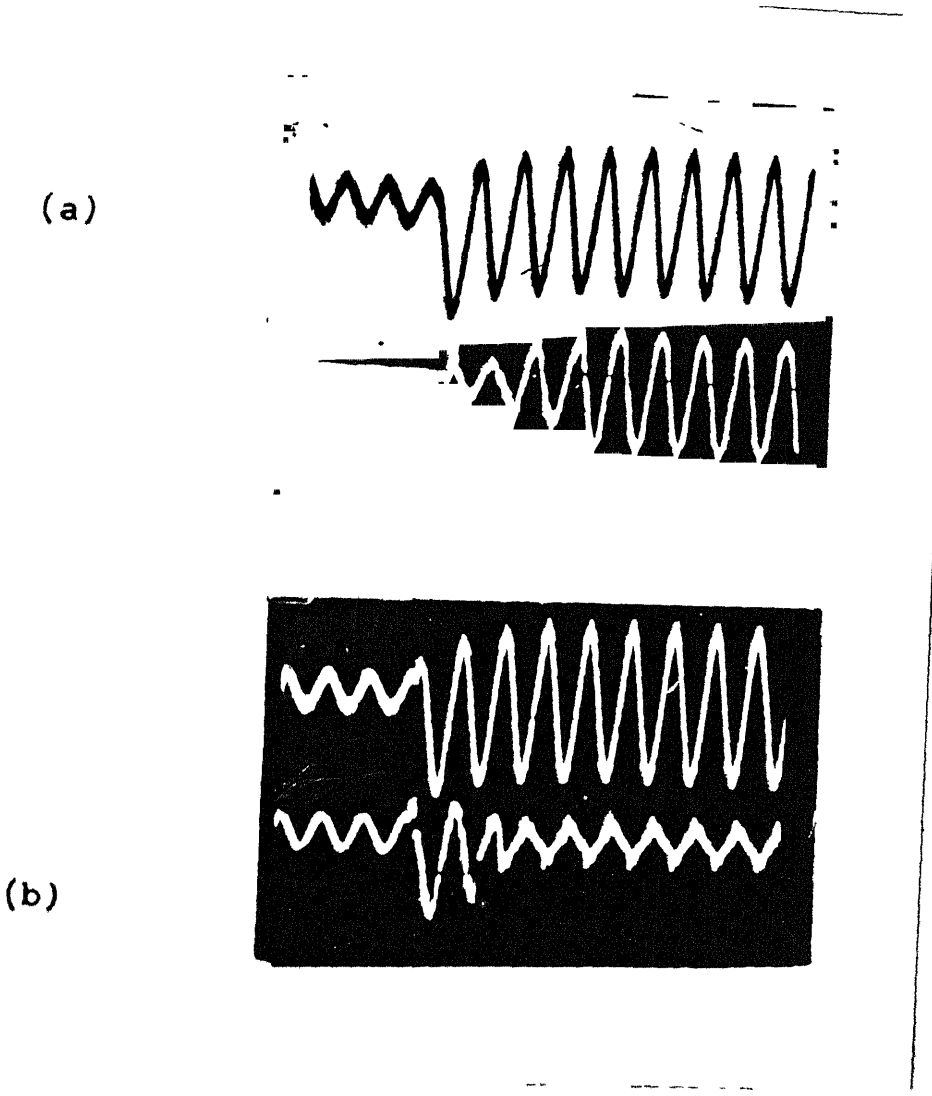


Fig. 7.8 TSC compensator transient response for load changing from highly resistive to highly inductive
(a) Top : Load current
Bottom : Compensator current
(b) Top : Load current
Bottom : Supply current

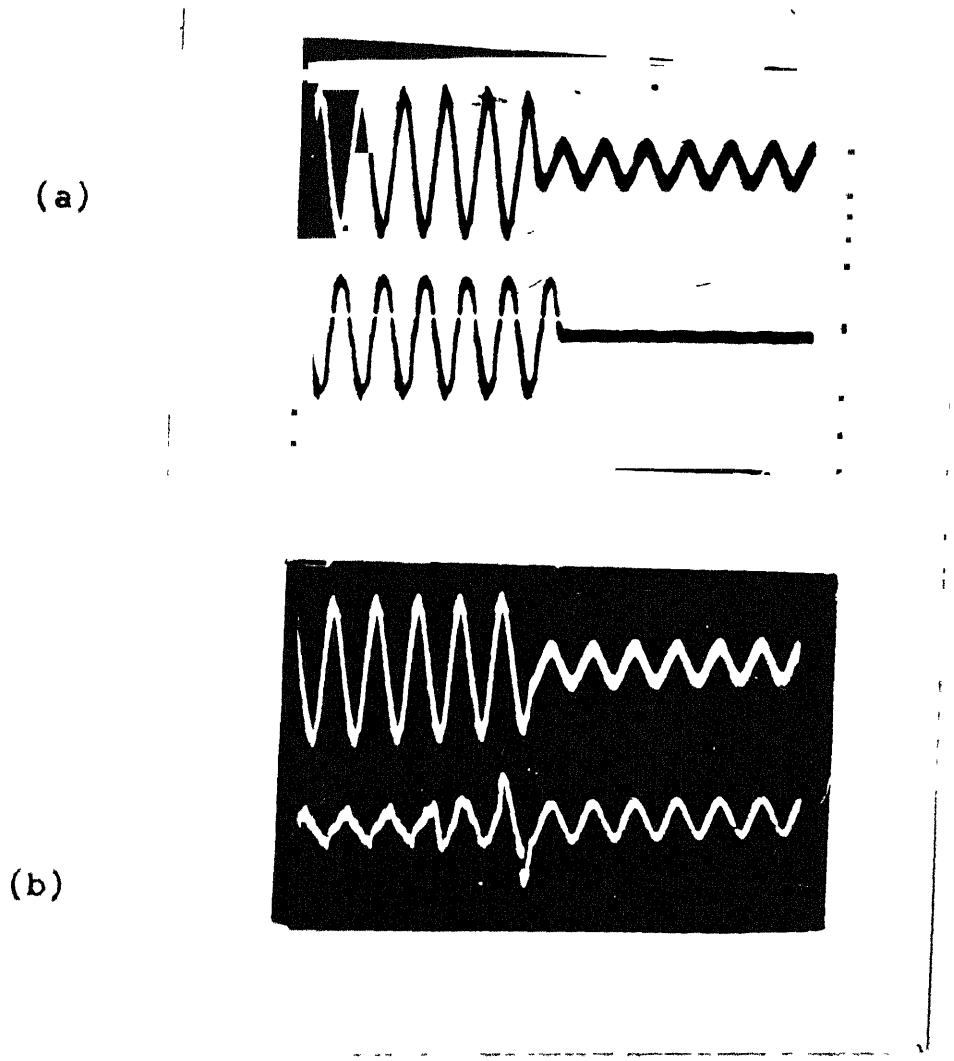


Fig. 7.9 TSC compensator transient response for load changing from highly inductive to highly resistive
(a) Top : Load current
(b) Bottom : Compensator current
(b) Top : Load current
Bottom : Supply current

7.3 POWER FACTOR CORRECTION BY FC-TCR COMPENSATOR

Fig. 7.10(a) shows the basic scheme for power factor correction employing FC-TCR type shunt compensator. As shown in the figure, the compensator basically consists of a fixed capacitor C in parallel with a thyristor switched reactor L.

7.3.1 Operating Principles

To keep the line power factor unity, the compensator current and the reactive load current should be of equal magnitude and opposite in phase. This requires that the compensator current should follow the variation of reactive load current.

Compensator current (capacitor plus reactor currents) may be controlled continuously by varying the reactor current with phase-control of thyristors. Fig. 7.10(b) shows the supply voltage and reactor current waveforms when the thyristors S_1 and S_2 are triggered at angle α in the positive and negative half-cycles respectively. The triggering angle α is measured from the zero of the supply voltage and varies in the range $\pi/2 \leq \alpha \leq \pi$. Thyristors turn off naturally at extinction angles β when current through them goes to zero.

The differential equation for reactor current, and, the initial conditions at the triggering instants are given by

$$\omega L \frac{di_L}{d\omega t} = E_m \sin\omega t \ , \qquad (7.5)$$

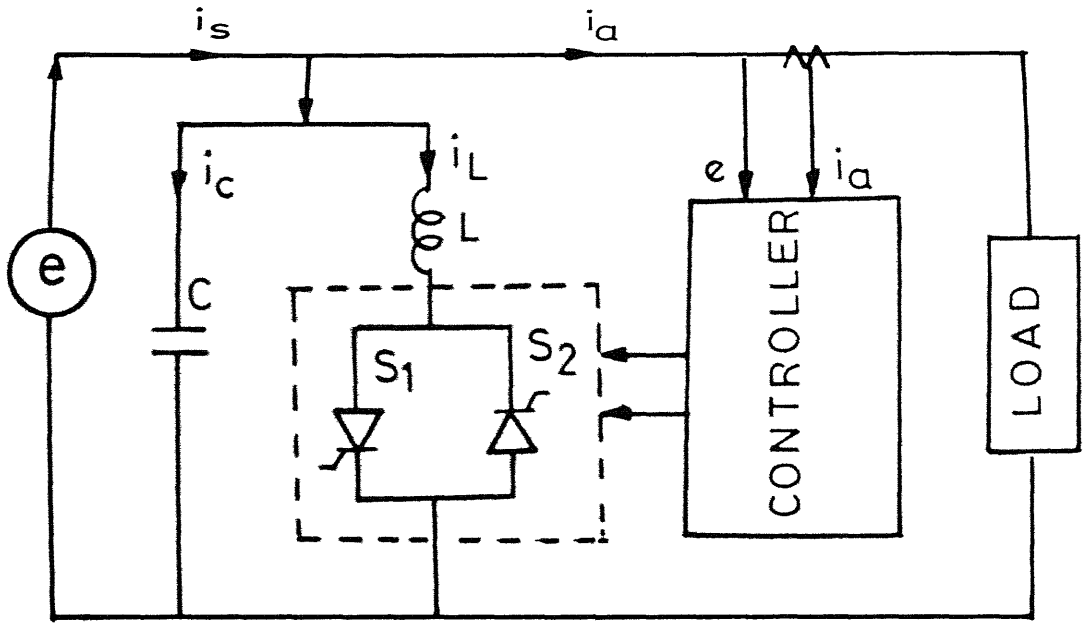
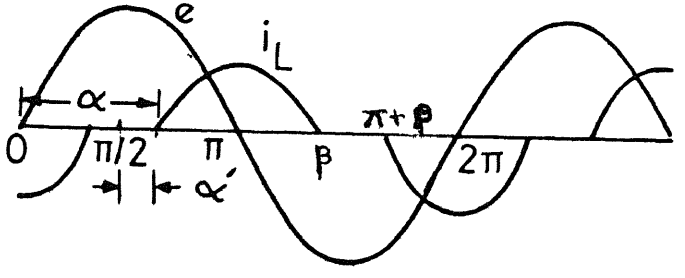


Fig.7·10(a) Basic FC-TCR type VAR compensator



and $\quad i_L = 0 \quad$ at $\quad \omega t = \alpha, \quad \pi+\alpha$

Solving eqn. (7.5), the reactor current is obtained as

$$i_L = I_L\,(\cos\alpha - \cos\omega t) \qquad \alpha \leq \omega t < \beta \qquad (7.6)$$

$$= I_L(\cos\alpha + \cos\omega t) \qquad \pi+\alpha \leq \omega t \leq \pi+\beta$$

where $I_L = E_m/\omega L \qquad (7.7)$

As seen from Fig. 7.10(b), reactor current is zero at the extinction angle β. Substituting this condition in eqn.(7.7), gives

$$\cos\alpha = \cos\beta$$

Since, $\alpha \leq \beta \leq 2\pi$, the above equation result in

$$\beta = 2\pi - \alpha \qquad (7.8)$$

The reactor current is almost sinusoidal and lags the source voltage by 90° when $\alpha = 90^\circ$, when commutation intervals of thyristors are neglected. The reactor current becomes discontinuous for $\alpha > 90^\circ$, and, the duration of zero current interval increases with an increase in firing angle. The reactor current may be expressed by Fourier series,

$$i_L = I_{L1}\cos\omega t + \sum_{n=2,3,\ldots} I_{Ln}\cos n\omega t \qquad (7.9)$$

where 'sin' terms are absent because of the waveform symmetry.

I_{L_1} and I_{Ln} are the fundamental and harmonic currents amplitudes which could be derived from the Fourier analysis of eqn. (7.6) as

$$I_{L_1}(\alpha) = -I_L[2(\pi-\alpha) + \sin 2\alpha]/\pi \tag{7.10}$$

$$I_{Ln} = \frac{4I_L}{\pi n(n^2-1)} [\cos\alpha \sin n\alpha - n\sin\alpha \cos n\alpha] \tag{7.11}$$

where $n = 3,5,7 \ldots$

The TCR current varies from its maximum value to zero when the firing angle α is varied from 90° to 180°. It may be more convenient to introduce a new firing angle α' which varies from 0° to 90° and measured from the peak of the supply voltage. α' is such that,

$$\alpha = \alpha' + \pi/2 \tag{7.12}$$

Substituting eqn. (7.12) in eqn. (7.10), the fundamental component of reactor current is obtained as

$$I_{L_1}(\alpha) = -I_L[1-(2\alpha'+\sin 2\alpha')/\pi] \tag{7.13}$$

Thus, the magnitude of the total fundamental current drawn by the compensator is

$$I_{CMPF}(\alpha) = I_C + I_{L_1}(\alpha) \tag{7.14}$$

$$= E_m[\omega C - \frac{1}{\omega L} (2\alpha'+\sin 2\alpha')/\pi] \tag{7.15}$$

where I_C = amplitude of the capacitor current

$$= \omega C E_m \tag{7.16}$$

If L and C are chosen such that $\omega L < \frac{1}{\omega C}$, it can be seen from eqn. (7.15) that the compensator current can be made net capacitive or inductive by controlling the TCR current.

The fundamental load current, with phase angle ϕ - which is taken as positive for leading power factor and negative for lagging power factor - may be expressed in terms of active and reactive components as follows :

$$\begin{aligned} i_a &= I_a \sin(\omega t + \phi) \\ &= I_a \cos\phi \sin\omega t + I_a \sin\phi \cos\omega t \\ &= I_{a\omega} \sin\omega t + I_{ar} \cos\omega t \end{aligned} \qquad (7.17)$$

where $I_{a\omega}$ = active load current amplitude

I_{ar} = reactive load current amplitude .

It is evident from eqn. (7.17) that the measurement of reactive load current in each half-cycle, as needed to control the compensator current mentioned earlier, can be obtained by sampling the load current at zero voltage crossings, i.e., $\omega t = 0, \pi, 2\pi$, etc.

The fundamental reactive source current is a sum of the reactive currents of the compensator and load. The amplitude of the fundamental reactive source current I_{SF} is obtained from the eqns. (7.14) and (7.17) and is given by

$$I_{SF}(\alpha) = I_{CMPF} + I_{ar}$$

$$= I_C + I_{L1}(\alpha) + I_{ar} \qquad (7.18)$$

For unity line power factor, the reactive source current must be zero. Therefore, from eqn. (7.18) the necessary condition that is to be satisfied for perfect compensation is :

$$I_C + I_{L1}(\alpha) + I_{ar} = 0 \qquad (7.19)$$

Equation (7.19) forms the basis for the control scheme described latter.

7.3.2 Selection of Compensator Parameters

The values of L and C of the compensator elements are dependent on the maximum values of reactive load currents to be compensated. If the reactive load current varies between the maximum limits of inductive value I_{lag} and capacitive value I_{lead}, then the compensator parameters are fixed on the following basis which keep the compensator cost and power losses low :

Let x be the ratio of maximum capacitive to inductive currents. Then,

$$x = I_{lead}/I_{lag} \qquad (7.20)$$

Normally, $x = 0$ for power factor correction of industrial loads and $x > 0$ for transmission line voltage correction and load compensation applications.

Load current maximum inductive :

At this limiting value, TCR current is made zero by keeping $\alpha' = \pi/2$ and the capacitor is sized to compensate the maximum inductive load current. For $\alpha' = \pi/2$ and $I_{ar} = -I_{lag}$ in eqn. (7.19),

$$I_C = I_{lag} \tag{7.21}$$

and

$$C = \frac{I_{lag}}{\omega E_m} \tag{7.22}$$

C smaller than given in eqn. (7.22) will result in under compensation.

Load current maximum capacitive :

At this limiting value, adjusting $\alpha' = 0$, TCR current is kept at its maximum value. Inductor is sized to compensate the maximum capacitive current of the load and the current due to compensating capacitor. For $\alpha' = 0$ and $I_{ar} = I_{lead}$ in eqn. (7.19) and using eqns. (7.20) and (7.22), the value of the inductance may be derived as

$$L = \frac{1}{(1+x)\omega^2 C} \tag{7.23}$$

The values of L and C chosen thus result in minimum rating of the compensator components. However, if C is over sized, then this also needs an over sized inductor, i.e., the value of L smaller than given by eqn. (7.23). It is evident from

eqn. (7.11) that for the same value of fundamental TCR current, the line current harmonics in the latter case are larger than the former one. Fig. 7.11 shows the harmonics variation with the TCR firing angle.

7.3.3 Basic Control Approaches for SVC

From eqns. (7.13) and (7.19), the basic laws governing SVC control may be dictated as

$$I_{L1}(\alpha) = -(I_C+I_{ar}) \qquad (7.24)$$

and

$$I_{L1}(\alpha) = -I_L[1-(2\alpha'+\sin 2\alpha')/\pi] \qquad (7.25)$$

The main objectives of the adopted control for reactive current control will be to determine the TCR current from the measurement of current due to compensator capacitor and load, and the corresponding firing angle α' from the steady-state characteristic equation of the reactor current. Three basic control approaches are generally employed for the control of SVC :

1. Feedforward control (FFC) :

This is a direct computational method which repeatedly solves a set of steady-state equations for the computation of required reactive current and the corresponding control angle α'. It is based on the fundamental presumption that the load is in steady-state between any two consecutive time instants at which the current in the compensator is changed. Between these

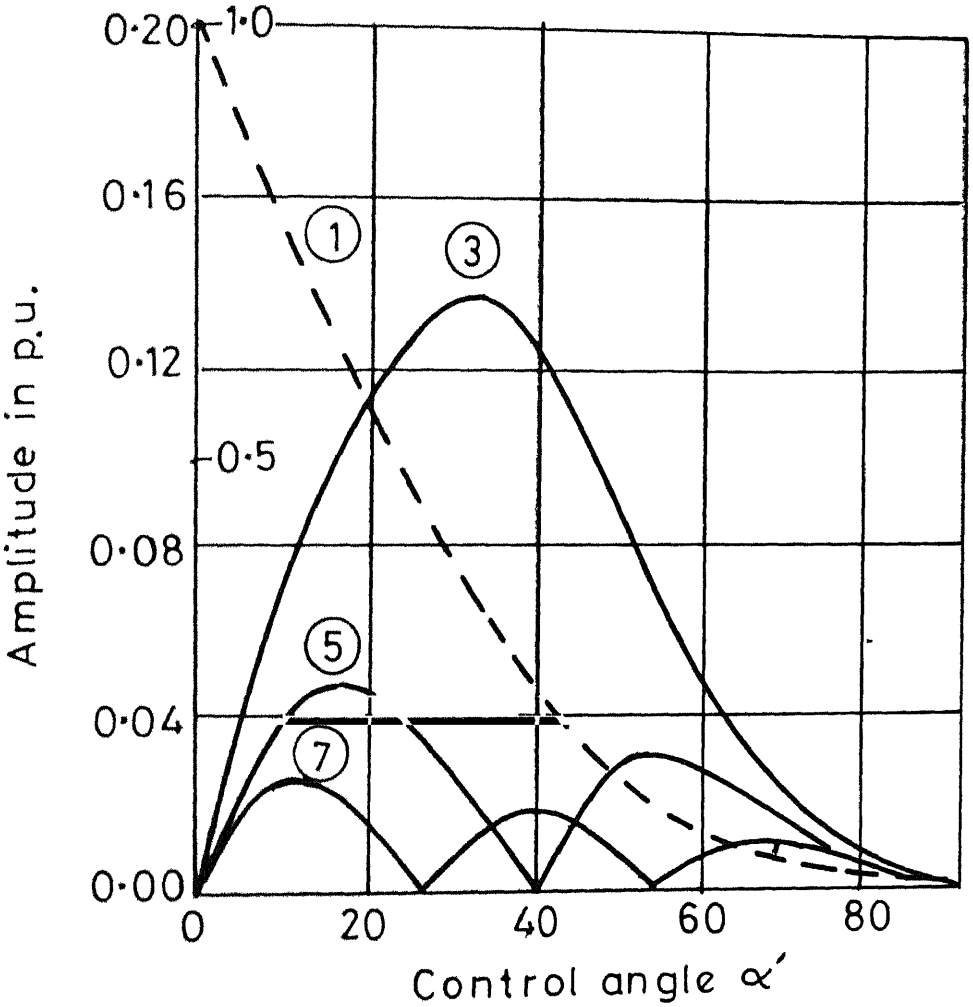


Fig.7·11 Harmonic currents generated by TCR

time intervals, the measurements and computations of the relevant quantities can be performed in each half-cycle of the supply wave. Feedforward control is fast and inherently stable because of open-loop control. This approach is normally suitable for control of load compensators only.

2. Feedback Control :

In this, to maintain some parametric value of the variable to be controlled at a desired level, the compensating current is controlled in a closed-loop. Feedback control is accurate and less sensitive to the changes in the parameters of the system to be controlled. Though this approach is mainly used for regulating the terminal voltage of the transmission network, it could also be used for load compensation of moderate response time.

3. Hybrid Control :

This is a combination of feedforward and feedback techniques. It combines the good features of both viz., fast response and better stability of the former, and better accuracy of the latter one. Hybrid approach may be used for load compensation as well as line voltage regulation.

7.3.4 Proposed Control Scheme

In SVC the compensating current can be adjusted at discrete instants of time, not more often than once in each half-cycle. FFC approach, normally applied to load and power factor

compensators due to its stable operation and fast response, works on the fundamental assumption that the load is in steady-state between any two consecutive instants of time at which the current in the compensator is changed. Then, the line current due to load and compensator capacitor may be expressed as

$$i_{ac} = (I_C+I_{ar}) \cos\omega t + I_{a\omega} \sin\omega t \qquad (7.26)$$

Between the time instants as stated above, current i_{ac} can be sensed for deriving the desired TCR current. In the case of normal FFC scheme the computation of desired reactor current and corresponding firing angle from the sensed current and the steady-state relations given in eqns. (7.13) and (7.26) involves repetitive computations in each half-cycle, in real time. This could be performed employing either a digital or an analog computation device. The former one has better control accuracy but it increases the system cost by high amount. Whereas, the latter one, which involves large number of discrete components for the realisation of various analog functions, is less accurate and more sensitive to the noise and temperature drifts.

In the following, a simple, accurate and cost effective FFC scheme for power factor correction is described. Unlike in the normal FFC scheme, in the proposed scheme, the desired reactor current and the firing angle in each half-cycle are readily available without going for the repeated computations.

In this the following strategies are adopted :

1. The desired reactor current as given in eqn. (7.24) is derived by sampling the current i_{ac} at zeros of the supply voltage.
2. For direct reading of firing angle, the nonlinear characteristic eqn. (7.25) is stored as a look-up table in the memory with firing angles as M bit memory data and the reactor currents as N bit memory addresses.

Fig. 7.12 shows the basic block diagram of the proposed scheme. Fig. 7.14 shows the details of signals operating on different blocks. To compensate the reactive component of current i_{ac}, the reactor current is controlled in the following manner. Current i_{ac} is rectified, and the rectified wave is sampled at zero crossings of the supply voltage to determine the magnitude of the uncompensated reactive current in each half-cycle. Current transformer (CT) and the harmonic filters in the secondary of CT may cause phase-shift in the fundamental current wave. The error due to this may be compensated by providing same amount of phase-shift to the sampling pulses. The sampled current, which corresponds to the magnitude of the desired reactor current, is digitized into a number of N bit wordlength using analog to digital converter (ADC). Digitized current addresses the memory to put the firing angle at the addressed location on the data

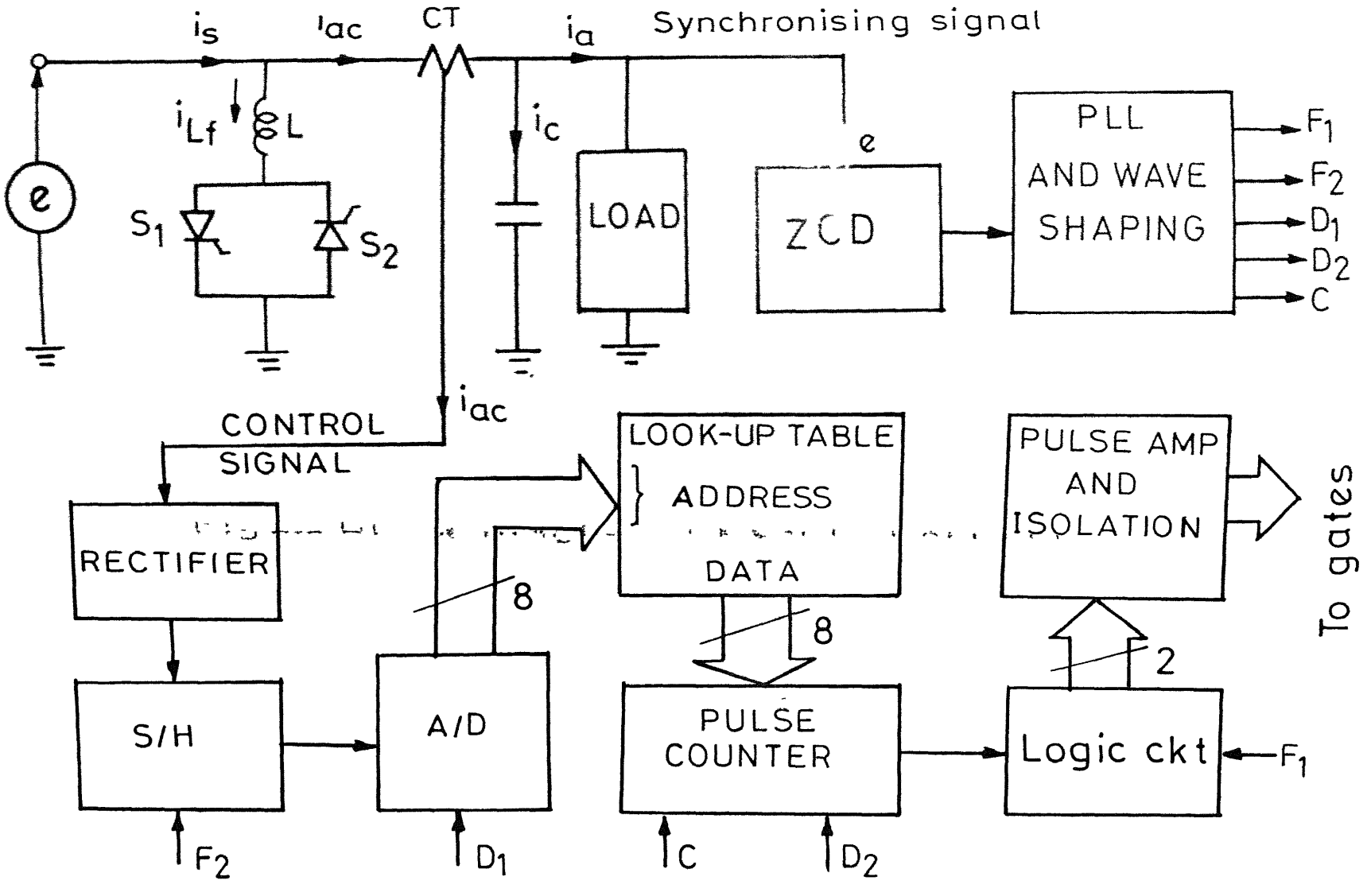


Fig.7.12 Block diagram of control scheme

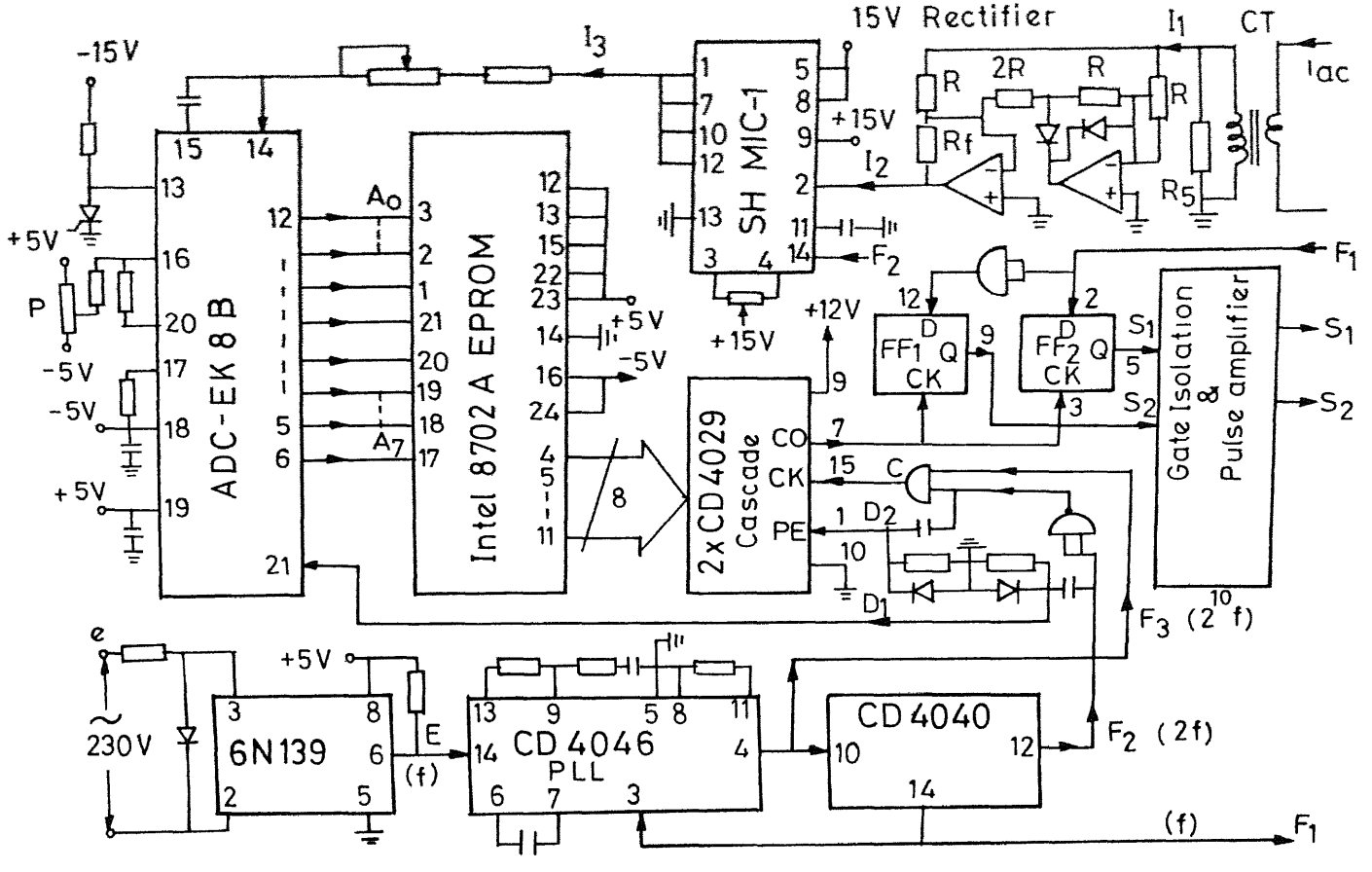


Fig 7.13 Control circuit diagram

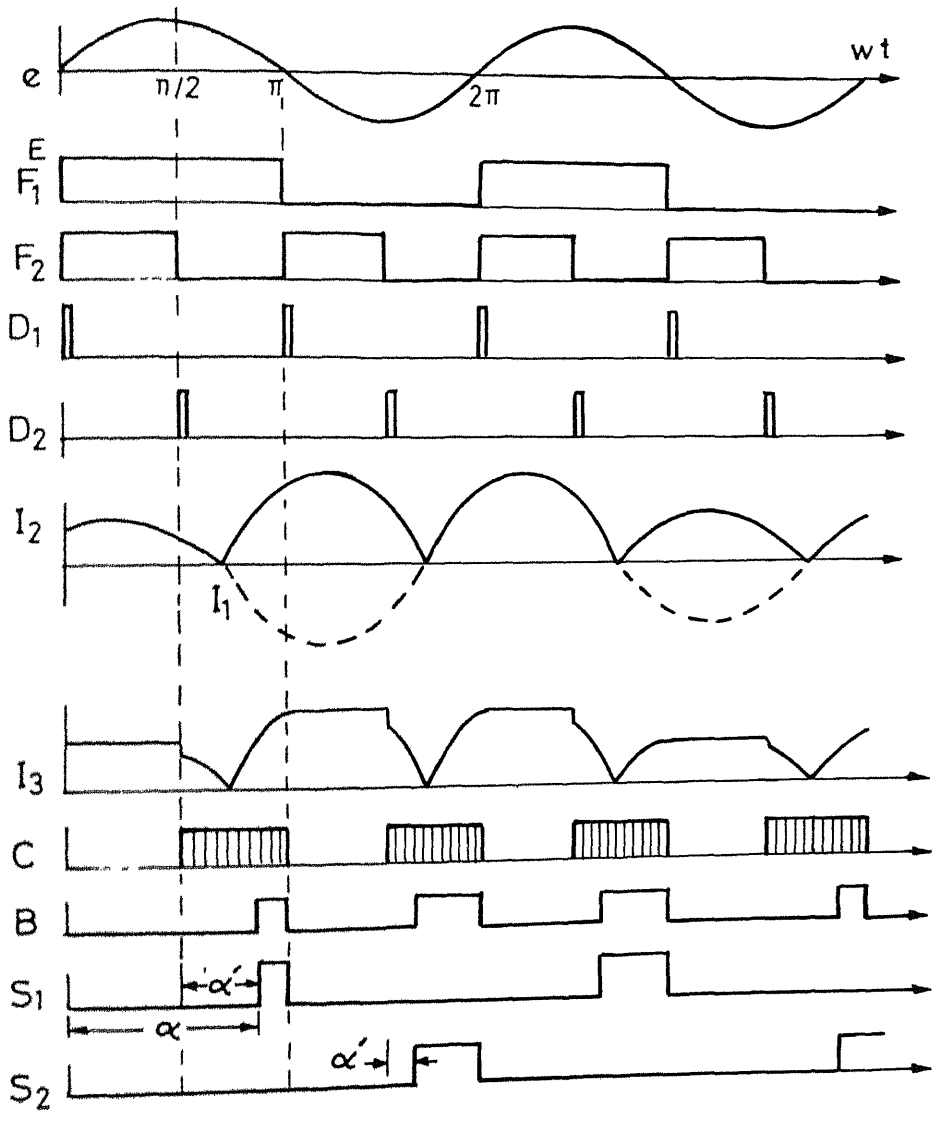


Fig.7.14 Timing diagram

bus which loads the M bit down counter with the desired firing angle. At the next peak of the supply wave, counter starts counting down at clock frequency f_{ck} and at the end of the count it generates the firing pulse at the desired instant.

Clock frequency f_{ck} is chosen on the following basis : The maximum count of 2^M corresponds to $\alpha' = 90^o$ and the count time T/4. Therefore, the clock frequency is given by

$$f_{ck} = \frac{4}{T} 2^M$$

$$= 2^{M+2}.f$$

where f = supply frequency.

7.3.5 Implementation of the Control Scheme

Proposed scheme has been implemented using all digital circuits. Figs. 7.13 and 7.14 show the detailed circuit diagram and the illustrative waveforms of the signals at different points in the circuit respectively.

Using opto-isolator, the supply voltage is digitised to generate a synchronised square wave E. Opto-isolator provides better isolation and prevents interaction between the power and control circuits. Control signals F_1,F_2 and F_2 of frequencies f, 2f and $2^{10}f$ respectively and synchronised to E are derived using PLL and modulo 10 counter in its feedback path.

The total current of the load and capacitor is sensed by a CT and rectified by a precision rectifier using operational amplifiers. On application of sampling pulse F_2, a sample and hold (SH MIC-1), samples the rectified wave at zero crossings of the supply voltage and holds it for 90°. The hold value corresponds to the reactive current demand. An 8 bit AD converter (ADC EK-8B) is used to convert the hold signal to a corresponding digital number. ADC starts conversion at each zero crossings by applying the pulse D_1 derived by differentiating F_2.

The nonlinear relation between the TCR current and the firing angle is stored as a look-up table in EPROM (8702A) having both address and data of 8 bit wordlength. Table 7.2 shows the contents of the look-up table. Output of the ADC

Table 7.2 Look-up Table

Current		Firing angle (α')	
P.U.	HEX (Address)	Degree	HEX (Data)
0.0000	00	90.00	FF
0.0039	01	77.94	DD
⋮	⋮	⋮	⋮
0.0392	0A	63.73	B7
0.0431	0B	62.85	B5
⋮	⋮	⋮	⋮
0.9960	EF	00.17	01
1.0000	FF	00.00	00

is connected to the EPROM address bus which gives the desired firing angle on the data bus.

At the peak of the supply wave, pulse D_2 loads the 8 bit counter (2xCD4029 cascaded) with the content of the data bus. D_2 has been derived by differentiating $\overline{F}_2$. Simultaneously, the application of clock C puts the counter into count down mode. C_2 of frequency $2^{10}f$ is derived by ANDing $\overline{F}_2$ and F_3. At the end of the count, counter generates a pulse B. A pair of 'D' flip-flops, with their 'D' inputs F_1 and $\overline{F}_1$, are clocked by pulse B. This generates two pulses S_1 and S_2 which after amplification and isolation are applied to the thyristor gates.

7.3.6 Experimental Verification

The control circuit discussed in the above section was constructed to verify the proposed scheme. Compensator performance was determined by compensating an inductive load. Load considered was a fixed inductor of 100 Ohms in series with a variable resistor of 250 Ohms supplied from 230 V, 50 Hz supply. The compensator parameters chosen were $X_L = X_C = 100$ Ohms.

Under steady-state operation the line power factor, with and without the compensator, was computed by measuring the line voltage, current and power. Line current and the computed power factor with and without the compensator are

tabulated in Table 7.3. This shows that with the compensator the line power factor remains close to unity over a wide range of the load current. Deviation of power factor from unity is due to the line current harmonics generated by TCR. At a high load current, i.e., high inductive load, the fundamental line current reduces to a very low value, whereas, the % harmonic content in the line current increases due to TCR current. Therefore, at the high value of the load current the line power factor deviates more from the unity value. Oscillogram in Fig. 7.15(a) shows the supply voltage and TCR current under steady-state operation.

Transient performance of the compensator was studied by suddenly changing the load parameters. During the transient period, the load current depends on the load parameters and the instant of occurrence of transient. Therefore, during the transient period, the load current may have a dc off-set. Oscillograms in Figs. 7.15(b) - (c) show the transient performance with various degrees of dc off-set in the load current.

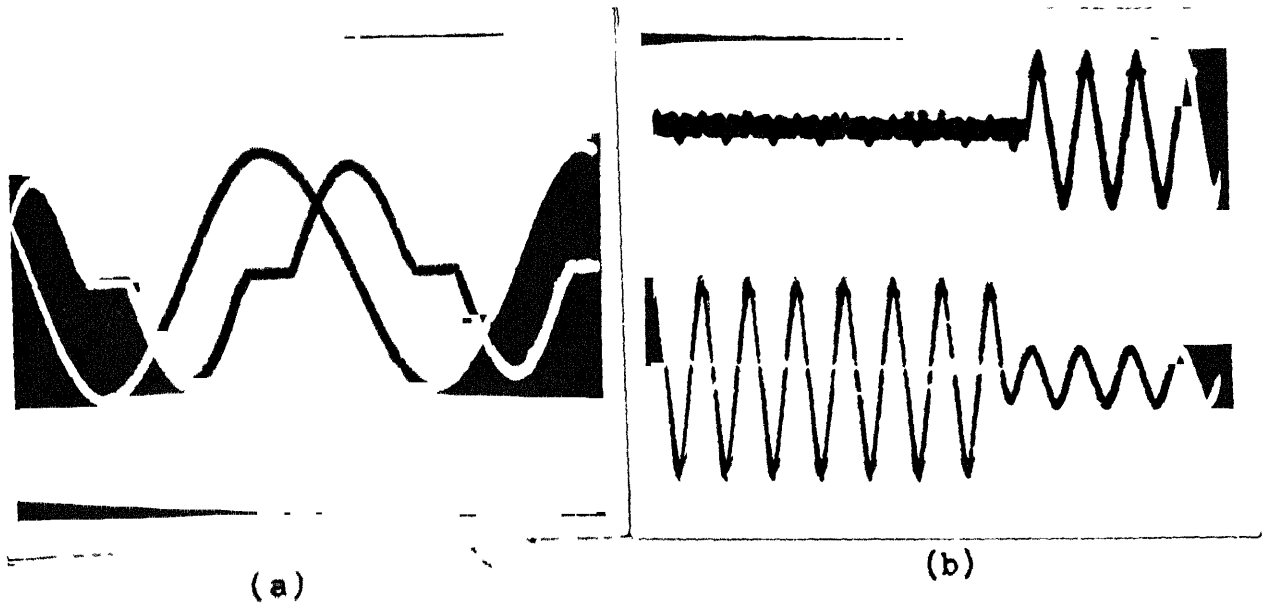
7.4 HARMONIC REDUCTION IN THE STATIC VAR COMPENSATOR BY SEQUENCE CONTROL OF TRANSFORMER TAPS

In the conventional approach, depending upon the system voltage, the thyristor controlled reactor in the static VAR systems is connected either to the line directly or to the fixed secondary of the step-down transformer. Line current

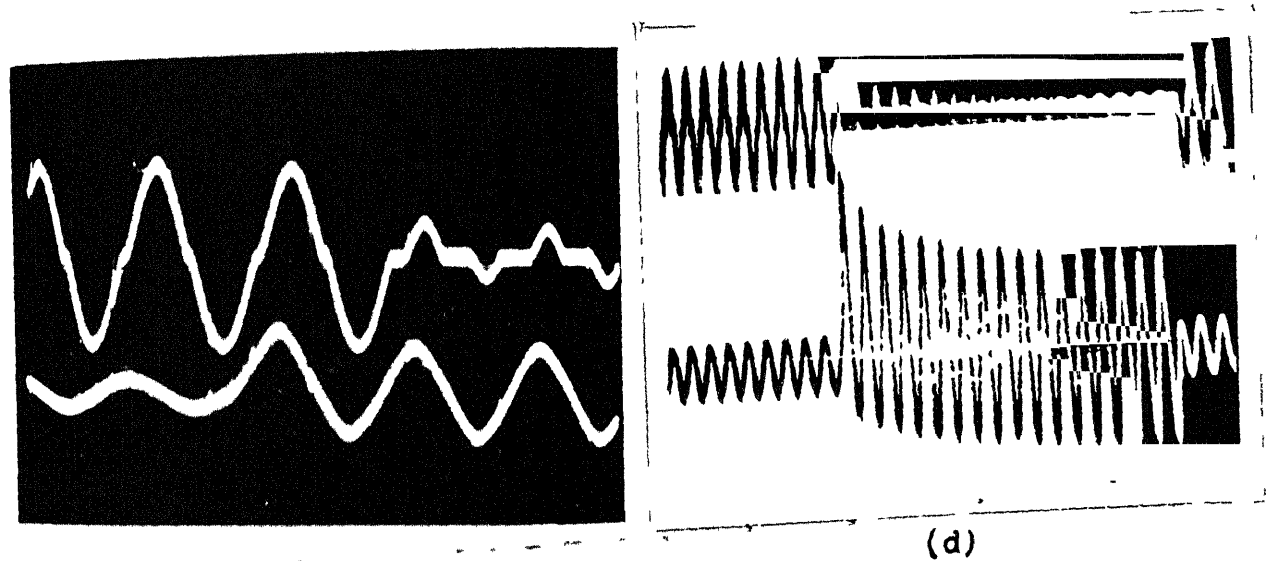
Table 7.3 Experimental values for FC-TCR compensator

Line voltage = 230 V

Without compensation			With compensation		
Line/load current Amp.	Power watts	p.f.	Line current Amp.	power watts	p.f.
1.0	193	0.839	0.94	208	0.962
1.2	215	0.779	1.02	248	0.980
1.4	240	0.742	1.10	251	0.995
1.8	226	0.545	1.05	240	0.993
2.0	196	0.426	0.92	208	0.982
2.2	129	0.255	0.74	145	0.850
2.3	25	0.047	0.27	30	0.483



(a) (b)



(c) (d)

Fig. 7.15 Oscillograms of the experimental results for FC-TCR compensator
(a) Steady state response supply voltage and TCR current
(b),(c),(d) Transient response
Change of load : (b) L to R, (c) R to L
(d) RL to L to RL
Top : TCR current
Bottom : Load current

harmonics due to discontinuous TCR current are relatively larger with the conventional control. From eqns. (7.10) and (7.11), for TCR operating on transformer secondary with secondary to primary ratio t_m, the amplitudes of fundamental line current I_1 and harmonic current I_{th} are given by

$$I_1 = I_m[2(\pi-\alpha) + \sin 2\alpha]/\pi \qquad \pi/2 \leq \alpha \leq \pi \tag{7.27}$$

$$I_{1h} = \frac{4I_m}{\pi n(n^2-1)} [\cos\alpha \sin n\alpha - n \sin\alpha \cos n\alpha] \tag{7.28}$$

where I_m= peak amplitude of the fundamental line current

$$= \frac{t_m^2 E_m}{\omega L} \tag{7.29}$$

and $n = 3,5, \ldots$

To reduce the harmonics,it is proposed to operate the TCR on variable voltage. Fig. 7.16 shows the power circuit to feed the reactor. It consists of a transformer having m taps on its secondary winding with secondary to primary ratios $t_1, t_2, \ldots, t_m$ ($t_1 < t_2, \ldots, < t_m$) and m thyristor-switch modules consisting of back-to-back connected thyristor pairs. Capacitor bank of the VAR compensator (not shown in the figure), depending upon its voltage rating may be connected to one of the m taps. Reactor L may be controlled

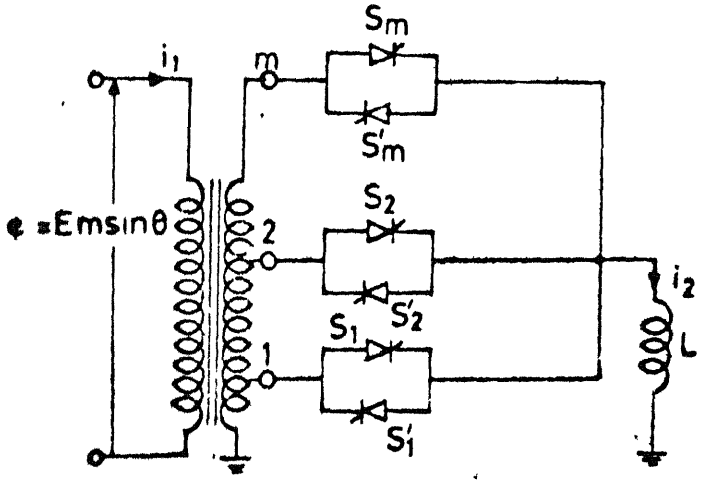


Fig. 7.16 Basic sequence control circuit (proposed method)

by changing the tap ratios in sequence and controlling the firing angle of the switch module of the operating tap. The amplitudes of the generated harmonics will depend on the operating sequence of the taps. In what follows, two alternative schemes for sequence control of transformer taps are described for control of fundamental line current over the full range.

7.4.1 Scheme-1

Let $\alpha_1, \alpha_2, \ldots, \alpha_m$ be the firing angles of switch modules 1 to m respectively. To vary the fundamental current from 0 to maximum value, reactor is supplied from tap 1 to tap m in sequence. Reactor is switched from the lower tap i-1 to the next higher tap i when the switch i-1 is in its full closure, i.e., $\alpha_{i-1} = \pi/2$. At switch over, the gate pulses to $(i-1)_{th}$ switch are blocked, whereas, i_{th} switch is switched on at $\alpha_i = \alpha_{ti}$ so that

$$I_1(\alpha_{i-1}=\pi/2) = I_1(\alpha_i=\alpha_{ti}) \quad i = 2,3, \ldots, m \qquad (7.30)$$

Now, the current is controlled by controlling the firing angle of i_{th} switch in the range, $\pi/2 \leq \alpha_i \leq \alpha_{ti}$.

At any time in a half-cycle, reactor current flows through one tap only. Therefore, the amplitudes of the harmonic currents depend on the tap under control. From eqns. (7.10) and (7.11), following equations may be derived for tap i :

$$I_1 = \left(\frac{t_i}{t_m}\right)^2 I_m[2(\pi-\alpha_i) + \sin 2\alpha_i]/\pi \qquad (7.31)$$

$$I_{1h} = \frac{4(t_i/t_m)}{\pi n(n^2-1)} I_m[\cos\alpha_i \sin n\alpha_i - n \sin\alpha_1 \cos n\alpha_1] \qquad (7.32)$$

I_{rh} = reactor current harmonics

$$= \frac{I_{1h}}{t_i} \qquad (7.33)$$

where $\pi/2 < \alpha_i < \alpha_{t1}$ (7.34)

and $i = 1,2, \ldots, m$

For the different taps, the transition angles α_{ti} are given below :

For tap 1, $\alpha_{t1} = \pi$

For tap $i > 1$, from eqn. (7.30)

$$\left(\frac{t_{i-1}}{t_m}\right)^2 = \left(\frac{t_i}{t_m}\right)^2 [2(\pi-\alpha_{ti})+\sin 2\alpha_{ti}]/\pi \qquad (7.35)$$

where $i = 2,3, \ldots, m$

Angle α_{ti} may be obtained from the numerical solution of eqn. (7.35).

Fig. 7.17 shows the conduction sequence of the taps for the typical case of three equally spaced taps on the secondary winding, when the fundamental reactive current varies over the full range. The control law is such that the gate pulses of the other thyristors, excepting that of the tap under control, are inhibited.

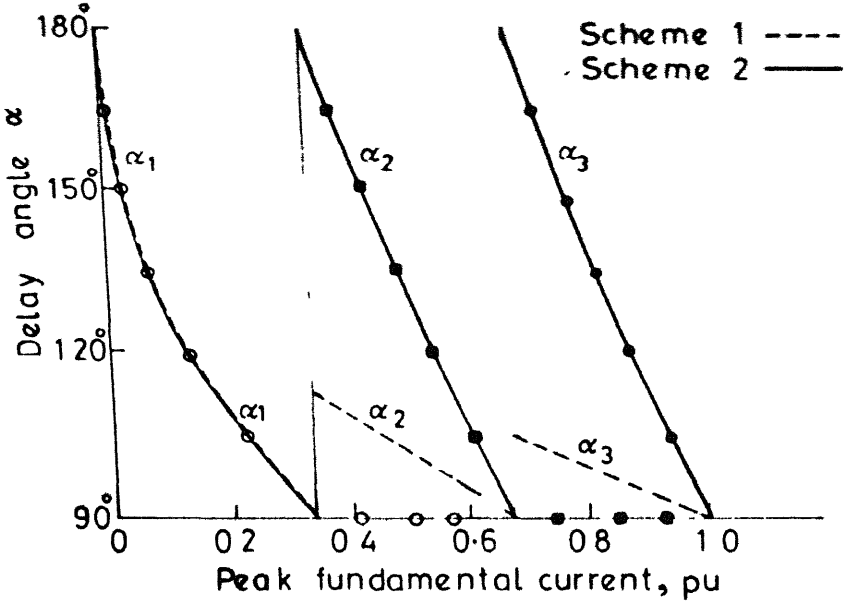


Fig. 7·17 Variation of delay angle with the reactive current demand in schemes 1 and 2 of the proposed method

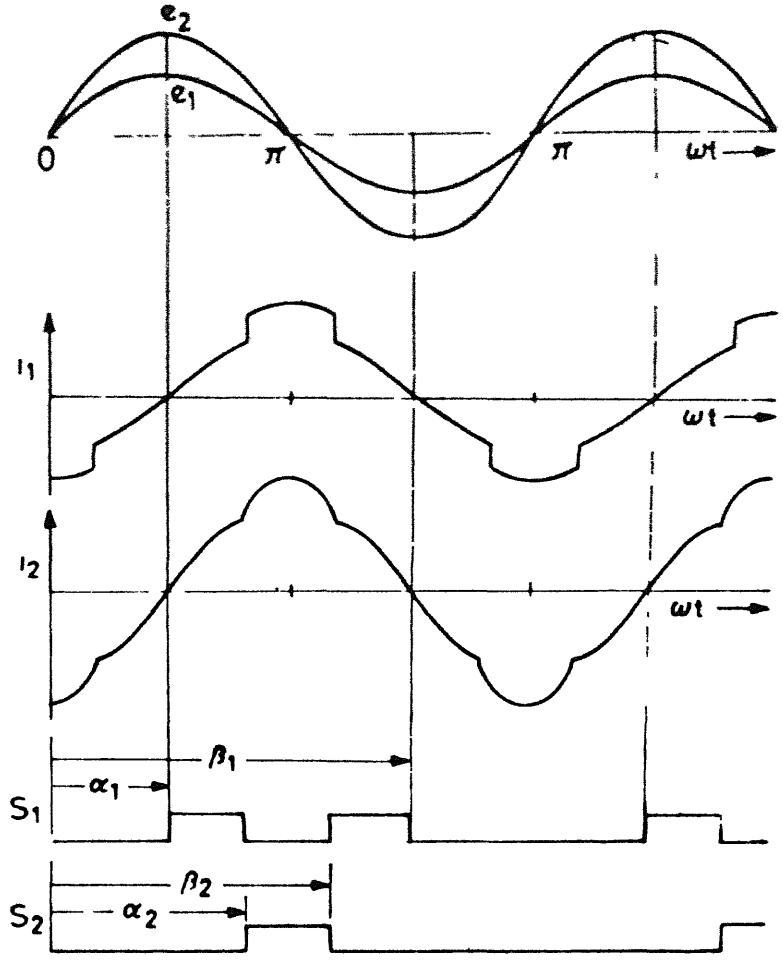


Fig.7·18 Taps voltages, line current, reactor current and gate pulses waveforms in scheme 2

7.4.2 Scheme-2

For control of the normalised reactive line current I_l/I_m over the full range $0 < I_l/I_m < 1$, the reactor, in the current ranges $0 < I_l/I_m < (t_l/t_m)^2$ and $(t_l/t_m)^2 < I_l/I_m < 1$, is operated in the following manner :

(a) For $0 < I_l/I_m < (t_l/t_m)^2$:

In this range, the reactor is connected to the tap 1 and the reactive current is controlled by controlling the firing angle α_1 in the range $\pi/2 < \alpha_1 < \pi$. For this range of control schemes 1 and 2 are the same. The relations given in eqns. (7.31) to (7.33), for i = 1, hold good for scheme 2 also.

(b) For $(t_l/t_m)^2 < I_l/I_m < 1$:

In this scheme, the current in the range $(t_l/t_m)^2 < I_l/I_m < (t_2/t_m)^2$ is controlled by controlling the adjacent taps 1 and 2. In general, in the range $(t_i/t_m)^2 < I_l/I_m < (t_j/t_m)^2$, control is affected by two adjacent taps i and j, where i = 1 to m-1 and j = i+1. Fig. 7.18 illustrates the operating principles, where e_i and e_j represent the voltages of taps i and j, i_1 and i_2 are the primary and secondary currents and, S_i and S_j are the gate pulses to the thyristors S_i and S_j of switches i and j respectively. In each half-cycle of the current wave, the reactor will be connected to taps i and j in the following sequence :

i) In the positive half-cycle of the reactor current, reactor is connected to tap i by triggering the thyristor S_i at $\alpha_i = \pi/2$.

ii) At $\omega t = \alpha_j$, tap j is more positive to tap i. Reactor is transferred from tap i to tap j by triggering S_j at α_j which, in turn, turns off S_i by placing reverse voltage $e_j - e_i$ on S_i.

iii) For the ideal reactor, the reactor current i_2 is symmetrical about $\omega t = \pi$. Therefore, i_2 at $\omega t = \alpha_j$ and β_j $(= 2\pi - \alpha_j)$ have the same values. At β_j, thyristor S_i is forward biased through S_j by voltage $|e_j - e_i|$. Hence, retriggering of S_i at $\omega t = \beta_j$ results in smooth transfer of reactor current from tap j to tap i by turning off S_j. At $\omega t = 3\pi/2$, current through S_i goes to zero which turns off S_i.

iv) In the negative half-cycle of current, thyristors S_i' and S_j' are operated similarly.

In general, for any two adjacent taps i and j that are operative in the range $(t_i/t_n)^2 \leq I_1/I_m \leq (t_j/t_m)^2$, the reactor current I_1 is controlled by controlling the firing angle α_j of tap j over the range $\pi/2 \leq \alpha_j \leq \pi$. Whereas, the thyristor switch of tap i is triggered at delay angle $\alpha_i = \pi/2$ and retriggered at $\alpha_i = 2\pi - \alpha_j$. During the intervals between $\pi/2$ to α_j, α_j to $2\pi - \alpha_j$ and $2\pi - \alpha_j$ to $3\pi/2$ the reactor current flows, respectively, through tap i, tap j and tap i.

7.4.2 .1 Line Current Harmonics in Scheme-2

The fundamental line current and the harmonic components for TCR operating on scheme 2 are derived as follows :

For $I_1/I_m < (t_1/t_m)^2$, only tap-1 is under operation. Therefore, eqns. (7.31) to (7.33) with i = 1 hold good for this scheme also. However, for $I_1/I_m > (t_1/t_m)^2$, each half-cycle of the current waveform is constructed by the current flow through the two adjacent taps i and j (= i+1) as shown in Fig. 7.18. Reactor current, in the different time intervals of half-cycle, is expressed as follows :

Reactor connected to tap i : $\pi/2 \leq \omega t \leq \alpha_j$

Reactor is switched to tap i by triggering thyristor S_i at $\omega t = \pi/2$. Hence,

$$\omega L = \frac{di_2}{d\omega t} = e_i = t_i E_m \sin\omega t \qquad (7.36)$$

With initial current $i_2(\pi/2) = 0$ in eqn. (7.36), reactor current is given by

$$i_2 = -\frac{t_i}{t_m^2} I_m \cos\omega t \qquad (7.37)$$

where $$I_m = \frac{t_m^2 E_m}{\omega L}$$

Reactor connected to tap j : $\alpha_j \leq \omega t \leq \beta_j$

Reactor is transferred from tap i to tap j by triggering thyristor S_j at $\omega t = \alpha_j$.

Hence, $$\omega L \frac{di_2}{d\omega t} = e_j = t_j E_m \sin\omega t \tag{7.38}$$

From eqn. (7.37), the initial condition

$$i_2(\alpha_j) = -\frac{t_i}{t_m^2} I_m \cos\alpha_j \tag{7.39}$$

From eqns. (7.38) and (7.39),

$$i_2 = I_m[(t_j - t_i)\cos\alpha_j - t_j \cos\omega t]/t_m^2 \tag{7.40}$$

Reactor connected to tap i : $\beta_j \leq \omega t \leq 3\pi/2$

Reactor is transferred back to tap i from tap j by triggering S_i at $\omega t = \beta_j = 2\pi - \alpha_j$.

Hence, $$\omega L \frac{di_2}{d\omega t} = e_i = t_i E_m \sin\omega t \tag{7.41}$$

From eqn. (7.40), the initial condition

$$i_2(\beta_j) = -\frac{t_i}{t_m^2} I_m \cos\alpha_j \tag{7.42}$$

From eqns. (7.41) and (7.42),

$$i_2 = -\frac{t_i}{t_m^2} I_m \cos\omega t \tag{7.43}$$

From eqns. (7.37), (7.40) and (7.43), the positive half-cycle of the reactor current is given by

$$i_2 = -\frac{t_i}{t_m^2} I_m \cos\omega t \qquad \text{for } \pi/2 \leq \omega t \leq \alpha_j \text{ and } \beta_j \leq \omega t \leq 3\pi/2$$

$$= I_m[(t_j - t_i)\cos\alpha_j - t_j\cos\omega t]/t_m^2 \quad \text{for } \alpha_j \leq \omega t \leq \beta_j \qquad (7.44)$$

where $\beta_j = 2\pi - \alpha_j$.

Line current, from eqn. (7.44), is given by

$$i_1 = -\left(\frac{t_i}{t_m}\right)^2 I_m \cos\omega t \qquad \text{for } \pi/2 \leq \omega t \leq \alpha_j \text{ and } \beta_j \leq \omega t \leq 3\pi/2$$

$$= I_m[t_j(t_j - t_i)\cos\alpha_j - t_j^2\cos\omega t]/t_m^2 \quad \text{for } \alpha_j \leq \omega t \leq \beta_j \qquad (7.45)$$

From the Fourier analysis of eqns. (7.44) and (7.45), the peak values of fundamental line current, line current harmonics and reactor current harmonics are given by

$$I_1/I_m = -[(t_j - t_i)^2 \sin 2\alpha_j - 2(t_j^2 - t_i^2)(\pi - \alpha_j)]/(\pi t_m^2) - (t_1/t_m)^2 \qquad (7.46)$$

$$I_{1h}/I_m = \frac{2}{\pi t_m^2}\left[(t_j^2 - t_i^2)\left(\frac{\sin(n+1)\alpha_j}{n+1} + \frac{\sin(n-1)\alpha_j}{n-1}\right) - \frac{2t_j(t_j - t_i)}{n}\cos\alpha_j \sin n\alpha_j\right] \qquad (7.47)$$

$$\text{and } \frac{I_{rh}}{I_m} = \frac{2(t_j - t_i)}{\pi t_m^2} \left[\frac{\sin(n+1)\alpha_j}{n+1} + \frac{\sin(n-1)\alpha_j}{n-1} - \frac{2}{n}\cos\alpha_j \sin\alpha_j\right] \quad (7.48)$$

where n = 3,5, ...

7,4.3 Performance Evaluation

The number of secondary tappings and their spacings have considerable influence on the amplitudes of the generated harmonics. Line and reactor current-harmonics have been evaluated for two and three taps having following turns ratios :

a) equally spaced taps, i.e., the tap ratios are selected as $t_i/t_m = i/m$ where i = 1,2, ..., m

b) unequally spaced taps with tap ratios $t_i/t_m = (i/m)^{1/2}$ where i = 1,2, ..., m .

Figs. 7.20 and 7.22 show the variations of the first few dominant harmonics in the line and the reactor currents with the fundamental current in p.u. of I_m.

Figs.7.20-21 show that, for the same number of taps, the choice of the tap ratios has a great effect on the magnitude of the harmonics. Choosing adequate number of taps and their ratios, the line current harmonics can be reduced to any desired extent. The optimum ratios to minimise a lower-order harmonic may be obtained as follows : From Figs. 7.20-7.21, it can be seen that over the full range of

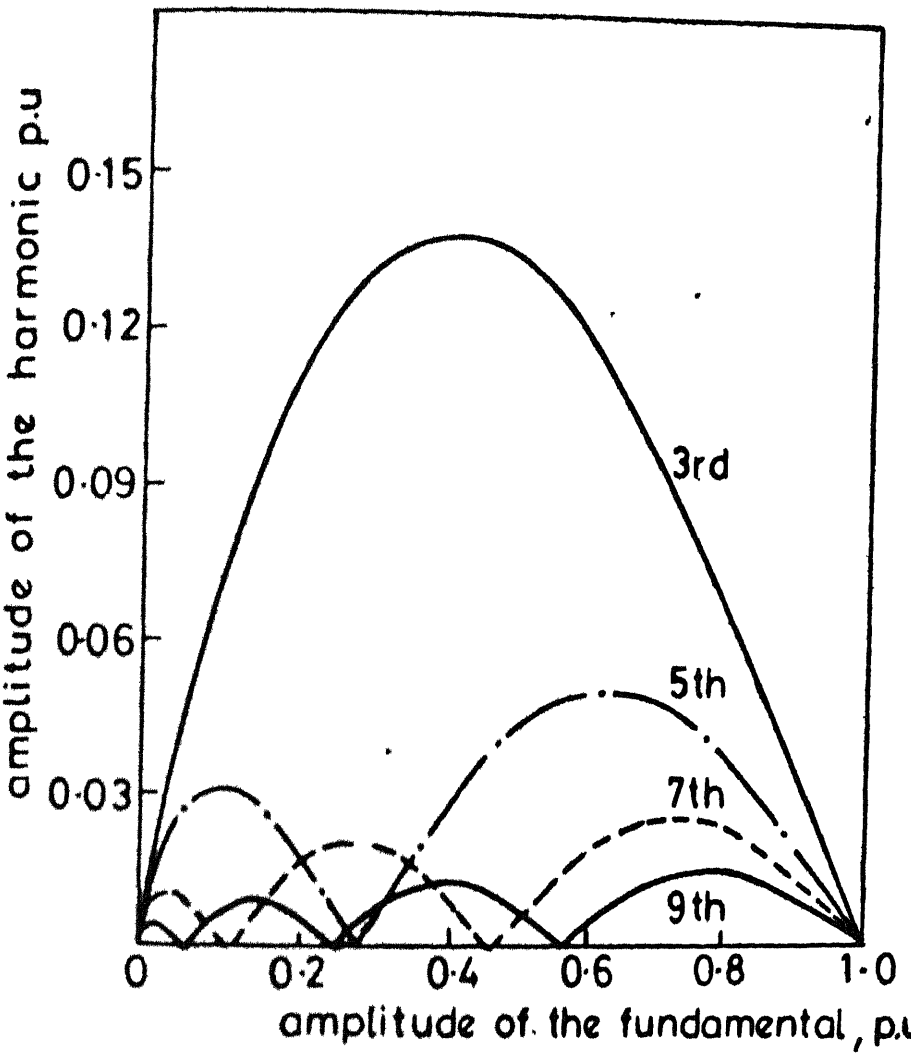


Fig.7.19 Variation of harmonic currents with the fundamental reactive current (conventional method)

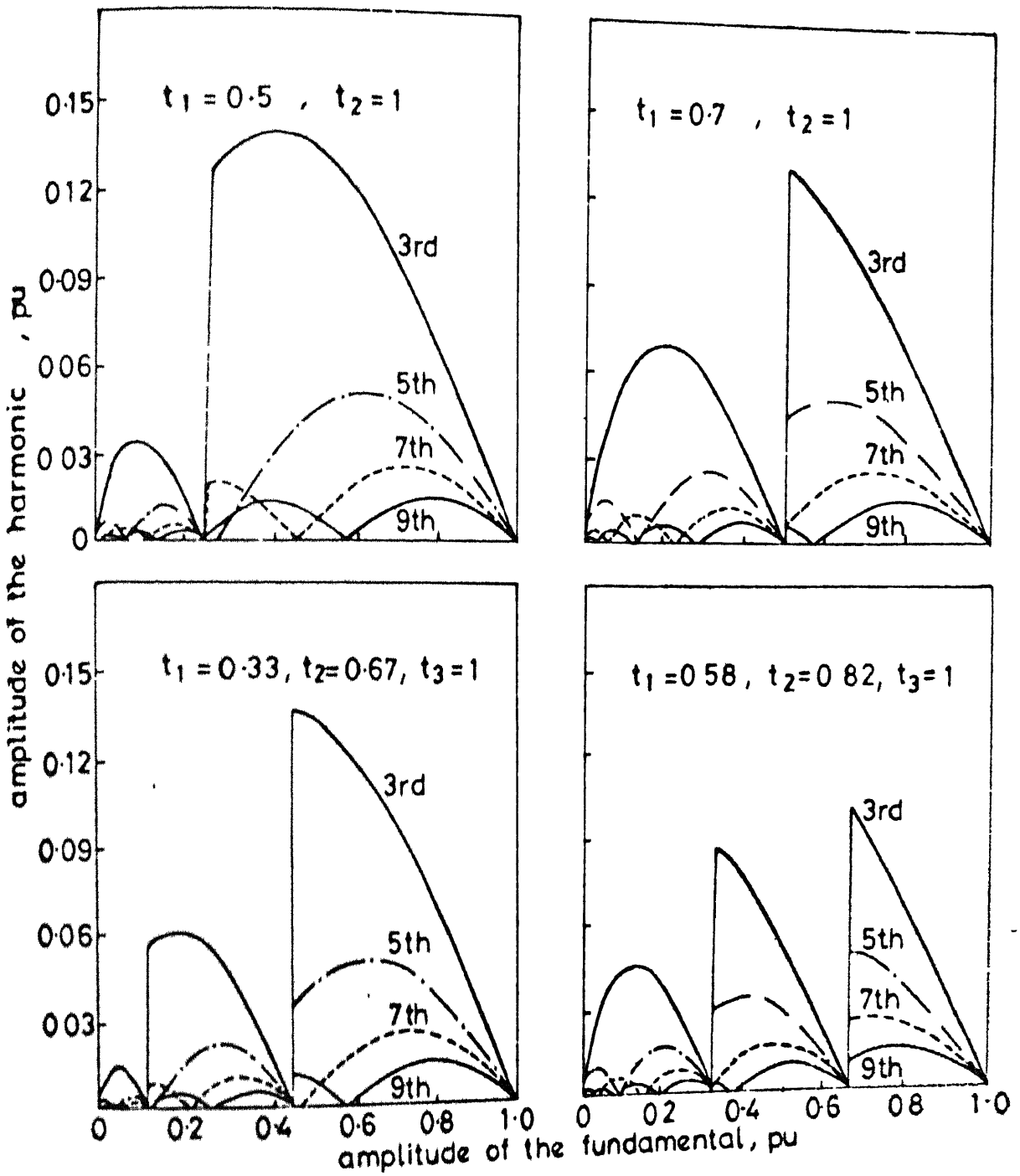


Fig.7.20 Variation of harmonic currents with the fundamental reactive current (proposed method)
Scheme 1

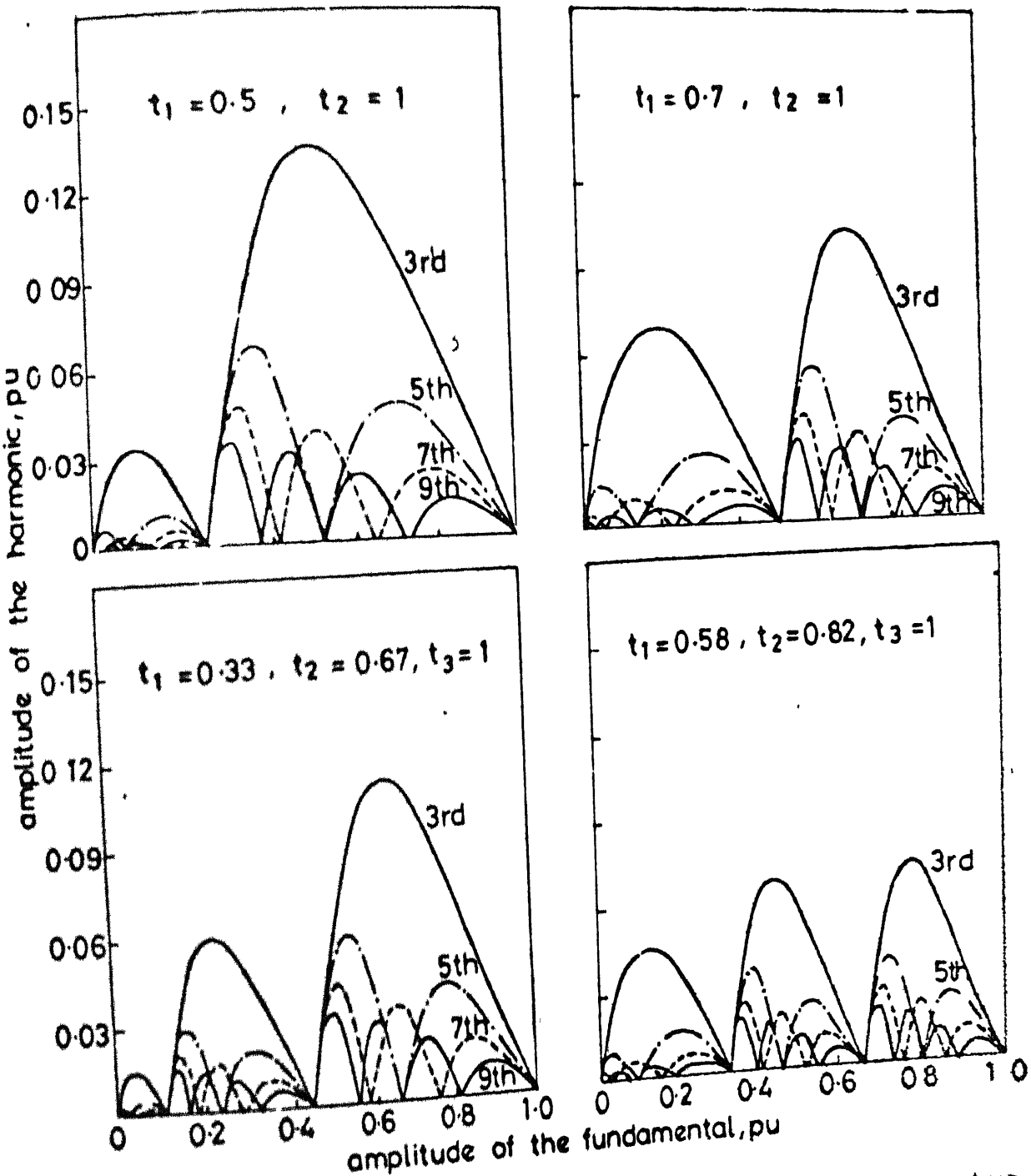


Fig. 7·21 Variation of harmonic currents with the fundamental reactive current (proposed method)
Scheme 2

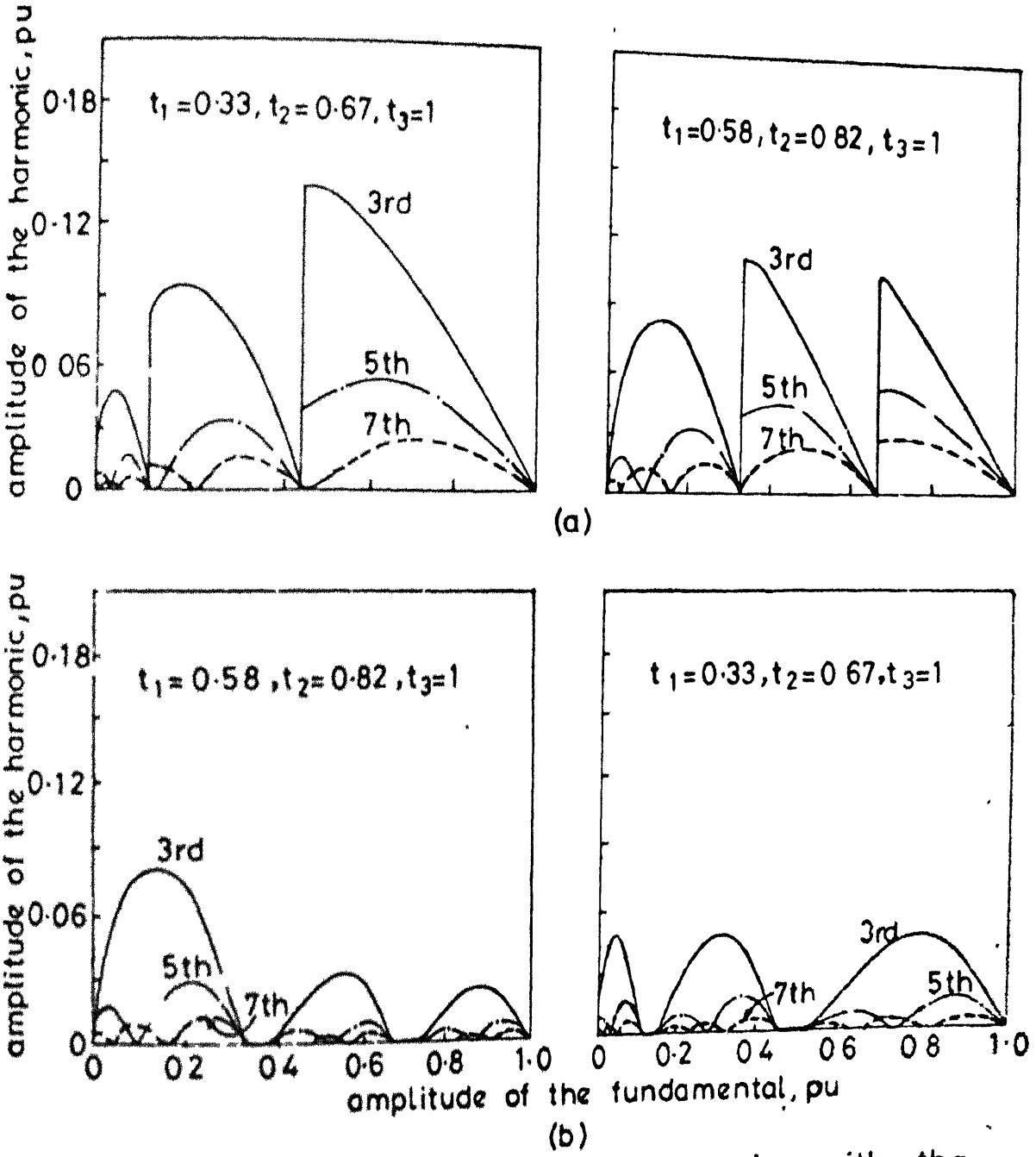


Fig.7·22 Variation in reactor current harmonics with the fundamental reactive current

(a) Scheme 1 (b) Scheme 2

fundamental current, 3rd harmonic has m peak values which are dependent on the tap ratios. The ratios obtained by equating the peaks will result in minimum 3rd harmonic.

7.4.4 Comparative Study of the Proposed Method and the Conventional Method

Fig. 7.19 shows the line/reactor current harmonics in the conventional method. From Figs. (7.19) - (7.22), following comparisons can be made between the conventional method and the schemes 1 and 2 of the proposed method.

i) In the present method, the line harmonics due to the TCR can be reduced to any extent by providing higher number of tappings on the transformer secondary. In particular, scheme 2 is more effective in reducing the line harmonics. This enables the use of small size filters for filtering of low-order harmonics. Whereas, in the conventional method the harmonics are uncontrollable within the compensator and, it requires relatively large-size filters for suppression of low-order harmonics from the line. In both the methods, the higher-order harmonics which may cause RFI may be suppressed from the line current by providing small size filters across the compensator terminals.

ii) In the proposed method, as the reactor current harmonics are low, reactor losses will also be low.

However, this method has the following disadvantages over the conventional one :

i It involves large number of thyristor elements of different voltage and current ratings. This may adversely affect the reliability of the compensator.

ii) The implementation of the control schemes is rather involved.

iii) In scheme 2 the current transfer from one tap to other tap takes place twice in each half-cycle. Hence, the switching losses in the semiconductor devices are increased. Whereas, switching losses in the scheme 1 and the conventional method are more or less equal.

7.4.5 Practical Realisation

The feasibility of both the schemes was verified experimentally for sequence control of two taps. Auto-transformer was used as variable ratio transformer. The reactor was rated for 2.5 KVAR when operated at 230V, 50 Hz supply. Brief description of the firing schemes for schemes 1 and 2 is given below.

Fig. 7.23 shows the block schematic of the firing schemes. Fig. 7.24 shows the timing diagram for Fig. 7.23. The necessary signals A to F, shown in Fig. 7.24, are derived by hardware realisations of different blocks, shown under common block. Logic blocks of scheme 1 and scheme 2 perform the logical operations on these signals to generate the required gate pulses. The control voltage v_c, controls the

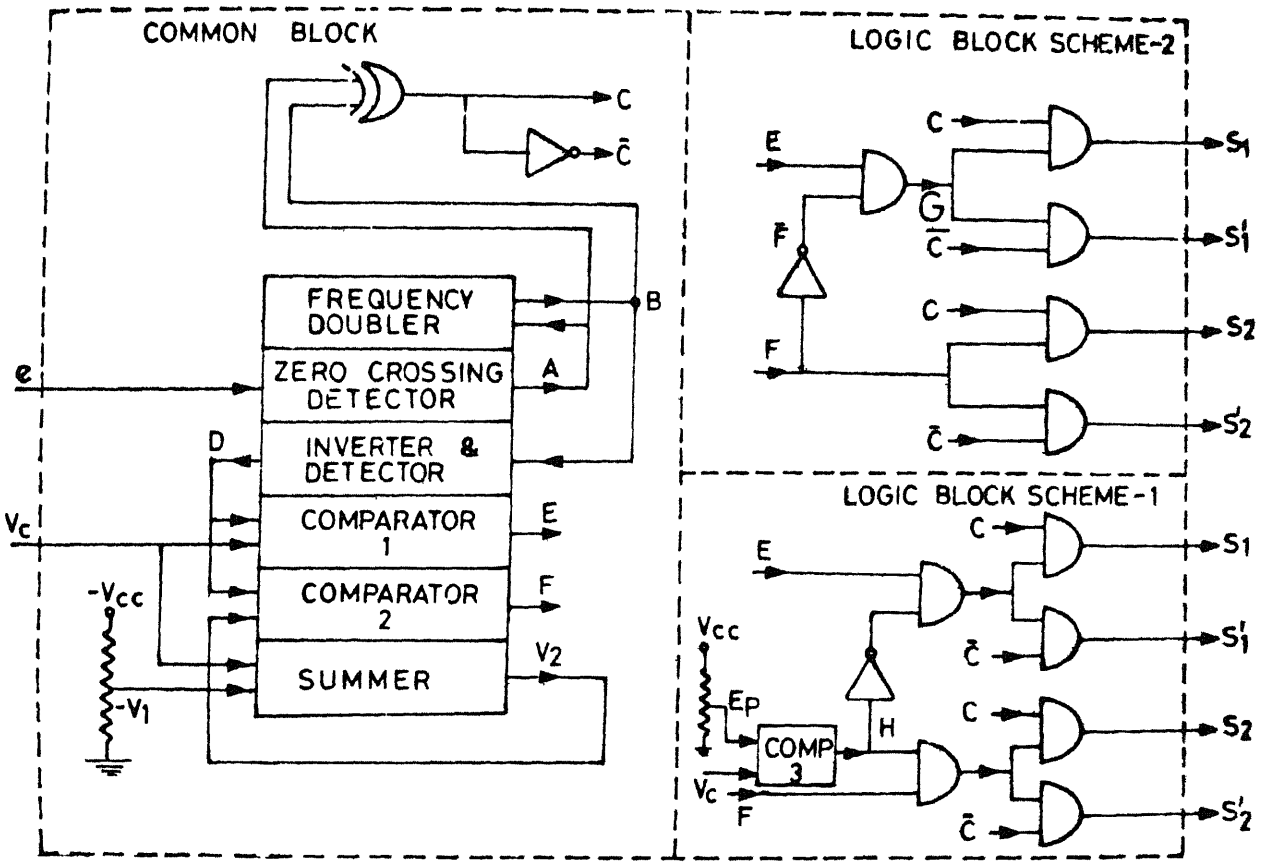


Fig. 7 23 Block schematic diagram of firing circuit for Schemes 1 and 2

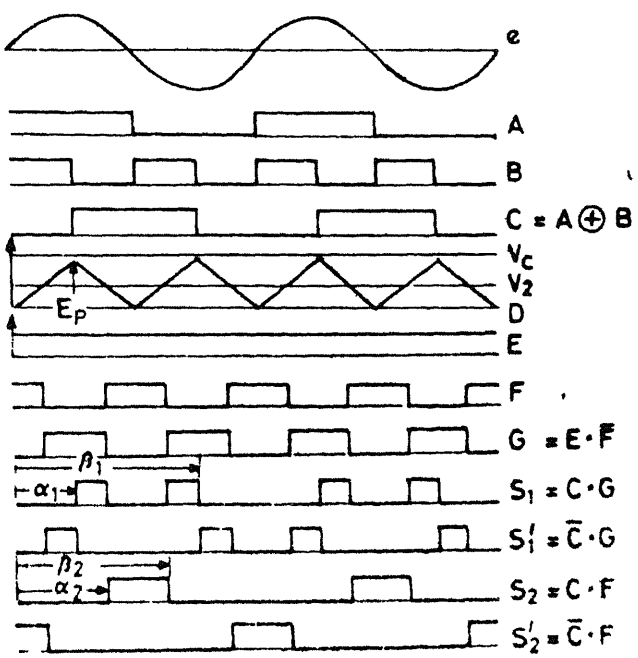


Fig 7·24 Timing diagram of Fig 7·23

reactive current. Comparator 1 operates on v_c and triangular wave D of amplitude E_p to control the firing angle α_1 of tap 1 Whereas, comparator 2 operates on v_2 and D to control the firing angle α_2 of tap 2.

where $v_2 = v_c - V_1$

and for scheme 1 $V_1 = (1 - \frac{\alpha_{t2}}{\pi}) E_p$

for scheme 2 $V_2 = E_p$

In scheme 1, when $v_c < E_p$, gate pulses are applied to the thyristors of tap 1, whereas the gate pulses to the thyristors of tap 2 are inhibited as the comparator 3 stays at low level. For $v_i > E_p$, comparator 3 enables the gate pulses to the tap 2 and, the gate pulses to the thyristors of tap 1 are inhibited. Varying the control voltage v_c from 0 to $(2 - \frac{\alpha_{t2}}{\pi}) E_p$, the reactive current varies from 0 to full-value.

Similarly in the scheme 2 for $0 < v_c < E_p$, gate pulses are applied to the thyristors of tap 1 whereas the gate pulses to the thyristor of tap 2 are inhibited due to low output of comparator 2. For $v_c > E_p$, comparator 2 gives output F which modifies the gate pulses to the tap 1 and applies the gate pulses to the thyristors of tap 2 shown in Fig. 7.24.

Fig. 7.25 shows the experimentally observed various waveforms in Schemes 1 and 2.

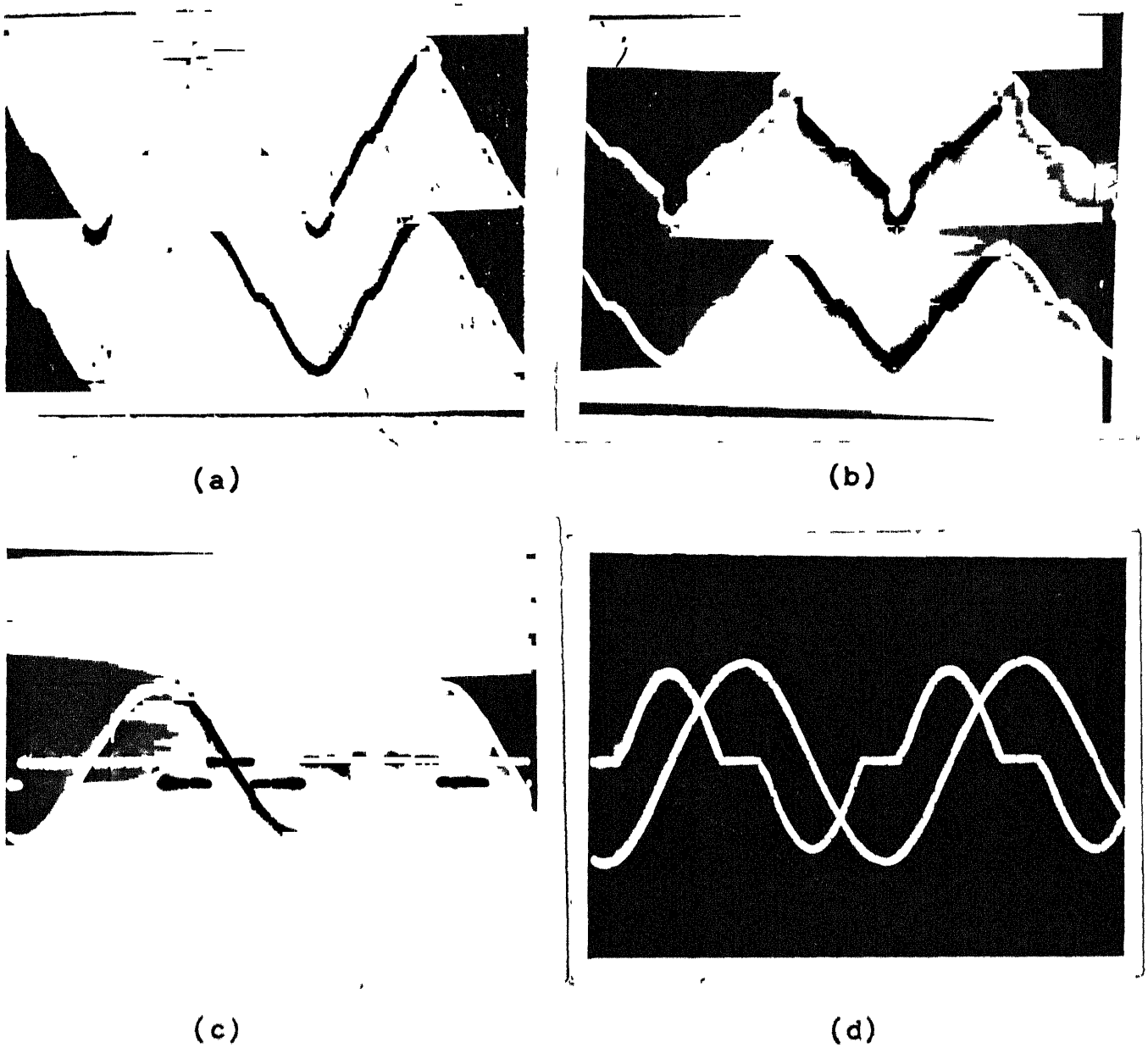
7.5 CONCLUSIONS

1. TSC Compensator

The principles of transient free switching of thyristor-switched capacitor are explained. A simple and reliable control scheme for power factor correction is proposed. The scheme has been realised for compensation of single-phase load with three capacitor banks and it has been shown that experimental and theoretical results agree satisfactorily.

2. FC-TCR Compensator

The principles of reactive power compensation with fixed capacitor thyristor-controlled reactor are described. A control scheme for FC-TCR type compensator for power factor correction is described. The scheme has been implemented using digital circuits having following features : inherently stable because of feed forward control; low cost and fast response because of look-up table approach; better accuracy and noise immunity due to digital circuits; compensation in each half-cycle with maximum time delay of half-cycle. The performance of the system has been examined experimentally which shows significant improvement in the system power factor over the expected range of load variation.



(a) (b)

(c) (d)

Fig. 7.25 Oscillograms illustrating TCR control with proposed schemes

(a) Scheme 2, $t_1 = 0.707$, $t_2 = 1$
Top : Line current Bottom : Reactor current

(b) Scheme 2, $t_1 = 0.5$, $t_2 = 1$
Top : Line current Bottom : Reactor current

(c) Line voltage and gate trigger pulses to thyristor of tap 1 in scheme 2

(d) Line voltage and line current in scheme 1

3. Harmonics reduction in TCR

Two sequence control schemes are described for reduction of line current harmonics due to TCR. Experimental results show the feasibility of implementing the schemes in practice.

CHAPTER 8

CONCLUSIONS

This chapter summarises the work done in this thesis. Few suggestions for further investigation are also included.

8.1 BRIEF REVIEW OF THE WORK DONE

In Chapter 2, eight prominent control schemes, namely, conventional phase-control, controlled flywheeling, extinction angle control and symmetrical pulse width modulation with one-pulse and two-pulse per half cycle, sinusoidal pulse width modulation and selective harmonic elimination are considered for comparison of single-phase ac-dc converters performance. The comparison is based on the performance criteria such as, line power factor, fundamental reactive power, line current harmonics, output voltage ripple etc. which are being computed assuming constant load current and ideal commutation. The study reveals that from the source consideration the extinction angle control with two-pulse/half cycle has the maximum third harmonic content. However, from the load consideration SPWM with two-pulse/half-cycle is the best due to lowest voltage ripple and the extinction angle control with two-pulse/half-cycle comes next. Whereas, the conventional phase control, from the source as well as load considerations, has the worst

performance due to constant amplitudes harmonic currents and high reactive power.

Further, the influence of pulse positioning and the number of pulses per half cycle on the motor performance has been studied for symmetrical and asymmetrical pulse-width modulations The comparison of the two schemes shows that they differ only at low pulse number. For higher pulse number, both have similar performance. Converter power factor with APWM scheme is of leading nature and this characteristic may be employed usefully for partial compensation of other inductive loads. The performance evaluation with higher pulse number shows that it shifts the dominant harmonics to higher order spectrum except that it has no influence on the other performance criteria.

In Chapter 3, an improved sequence control for natural commutated series connected ac-dc bridge converters is described. For improvement of input and output performance, the series connected bridges are rated for optimum values and they are controlled with half-controlled characteristic. Two alternative sequence control strategies are described to keep the maximum reactive power of the converter system below that of minimum rated bridge. A generalized method for determining the bridge ratings is described. The performance comparison shows good improvement in the input and output characteristics over the other schemes.

A selective harmonic elimination scheme, employing odd number of pulses/half cycle, is described in Chapter 4 for elimination of any one or any number of unwanted line current harmonics in forced-commutated ac-dc converter. Waveform symmetry of the line current with respect to the supply voltage keeps the displacement factor at unity. Present method employs 2M+1 pulses/half cycle to eliminate M harmonics. Pulse locations depend upon the order of the harmonics to be eliminated. Elimination of third, third and fifth, third, fifth and seventh harmonics is considered. Comparison with the alternative arrangement employing even number of pulses/half cycle shows that the proposed methods have higher control range and lower dominant harmonics. Control circuit, for rectification as well as inversion operation of self-commutating bridge [17] with the present scheme is described. Experimental investigation conform the operation of the scheme as predicted theoretically.

In Chapter 5, a comparative study of different control schemes of single-phase ac controllers feeding a resistive load is made for maximum of two forced-commutations per half cycle. Comparison is based on the performance criteria such as line power factor, displacement factor, distortion factor and line current harmonics. The control scheme considered for comparison are phase-control, extinction angle and symmetrical pulse-width modulation schemes with one- and two-pulse/half-cycle and sinusoidal pulse-width modulation. Comparative study shows that

sinusoidal PWM has lowest third harmonic current while highest fifth harmonic current : SPWM and extinction angle control schemes with two-pulse have the highest third harmonic content. Hence, for single-phase and three-phase four-wire loads, from the consideration of line harmonics, sinusoidal PWM is the best. Whereas, for delta connected load,with thyristor-switch in series with each phase, phase-control and single-pulse extinction control schemes are the best. Line power factor is same for each scheme which shows that higher order harmonics increases while reducing lower order harmonics.

In Chapter 6, first a scheme for selective harmonic elimination in ac controller feeding resistive load is described. It employs 2M+1 pulses/half cycle to eliminate M unwanted line current harmonics. Pulses are located symmetrically about $\pi/2$ axis of supply voltage and their locations are fixed depending upon the harmonics to be eliminated. Because of the fixed pulse-locations realization of control scheme is simple. Power and control circuits for realization of the schemes are described. Experimental investigation to confirm the feasibility of the proposed scheme is done. Experimental results shows that the circuit operation is as predicted theoretically.

Next, a control scheme for reduction of any one line harmonic in ac controller feeding resistive load is considered. Present scheme employs three pulses of equal widths per half-

cycle. Pulse positions are determined by equating harmonic coefficient corresponding to flat-topped current waveform to zero. As the actual line current consists of sinusoidal segments, fixing of the pulses assuming constant line current waveform does not eliminate the desired harmonic completely but reduces it to a very small value. Proposed scheme is compared with the alternative scheme which employs two pulses/half cycle. Superiority of the proposed scheme over the other one with regard to lower dominant harmonic and higher control range is established.

Dynamic compensation of reactive power is considered in Chapter 7. A control scheme for transient free switching of capacitor banks in thyristor-switched compensator for power factor correction of inductive loads is described. Next a digital control scheme for fixed capacitor thyristor-controlled reactor type compensator for power factor improvement is described. Circuit realization is simplified using look-up table approach. Then a sequence control technique for thyristor-controlled reactor is described to reduce the harmonics generated by TCR in the static VAR compensators. Two alternative schemes are given and the experimental results show that the circuit operation is as predicted theoretically.

8.2 SUGGESTIONS FOR FURTHER WORK

The present work may be extended further in the following areas.

1. The harmonic elimination principles discussed in this thesis may be applied to three-phase ac-dc converters and ac-controllers.
2. Assuming pulse widths and pulse locations varying, a generalized algorithm may be derived for elimination of line current harmonics in the thyristor converters. Turn on and turn off angles of the pulses may be stored in the semiconductor memory as look-up table and the algorithm may be realised using microprocessor.
3. For reduction of the TCR harmonics, an optimum turns ratios may be determined by equating, over the operating range, the peaks of the harmonics to be minimized. TCR performance may be investigated using this ratio and the control strategies described in this thesis. Further investigations may be made applying simultaneous control to all the taps with the optimum turns ratios.

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3. Publications :

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i) H.K. Patel and G.K. Dubey, 'Modified sequence-control technique for improving the performance of regenerative bridge converters', IEEE Trans. Ind.App., vol. IA-19, Sept/Oct. 1983, pp 682-689.

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